


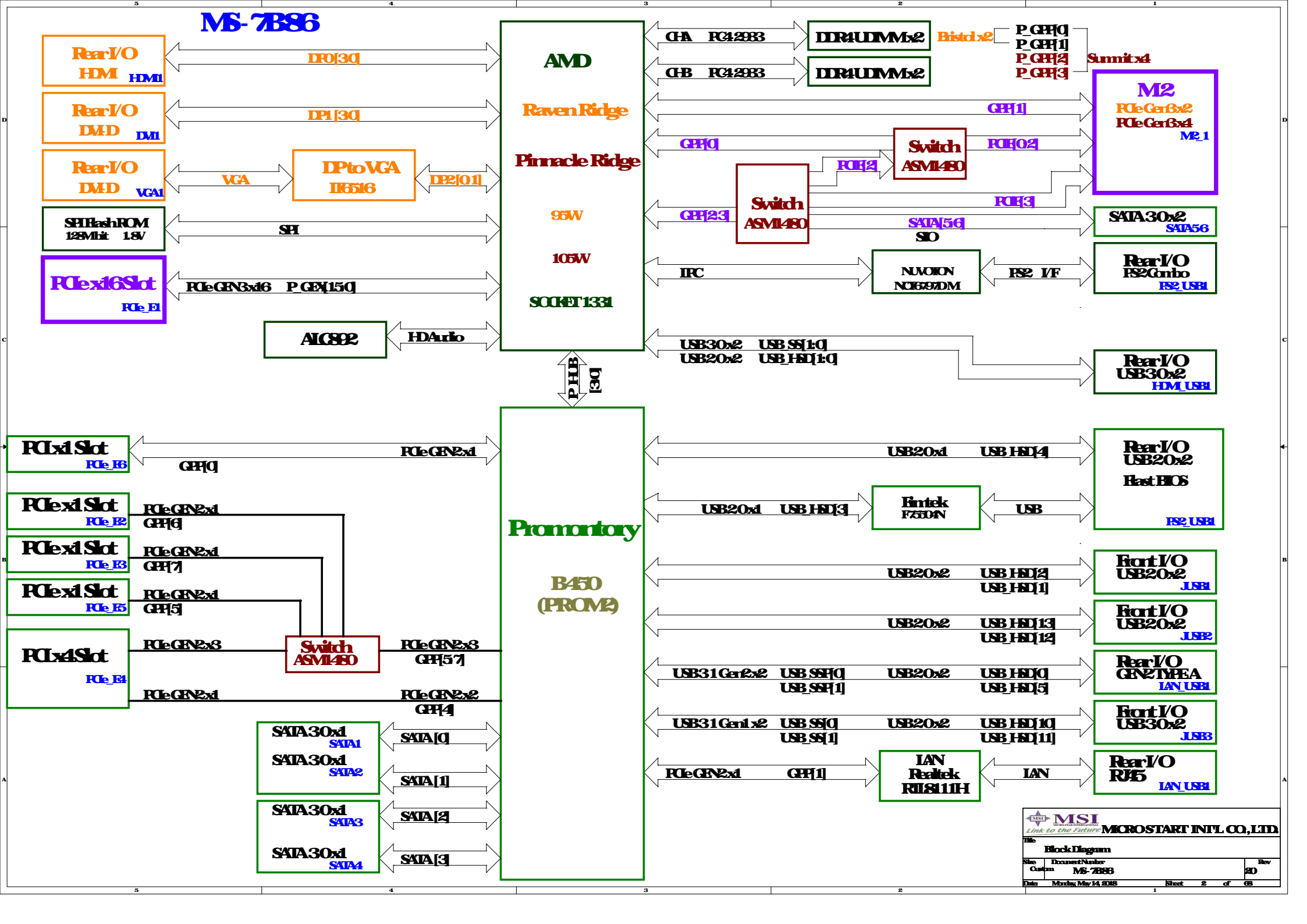


01 CoverSheet	39SATA
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03FM1DDR4IF	41HDM
04AM1PCIE/SATAE	42ACPI5VDIMM3/5B
05AM1Display/Audio	43DDR VPP25VTT
06AM1SVI/ACPIGPIO	44DDR Power RI8125E
07AM1IPC/SPI/USB/CLKSTRAP	45CPU Power RI88044:2
08AM1Power/VDDIO_AUDIO Power	46/47CPU Phase1-5
09,10RIC/Clear CMOS/RIC Power/GND	48/49CPUNB,CPUNB_S5
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15Promontory-PCIE/SATA/SATAE	51CPU PowerVDDP- MP8712
16Promontory-USB/OC	52PromGS71332.5V
17Promontory-CLK/ACPI/GPIO	53Prom SY8288RAC / 1.05V
18,19Promontory-Power GND	54VRMEN/PWRGD
20PCI_E1/E4_X16	55RI9553B CURRENT SENSE/OV Control
21 PCI_E2_E3_E5/E4_X1/X4	56ATXFront Panel
22PCIE Switch_X4/X1/X1	57ALLIED Control
23PCIE Switch_M2_2SATA	58TEMP SENSOREM CAP
24SIONCI679D	59IEDMCU Control
25SIOHMMCOM	60Power/JPIPE
26M2_1	61JLED1/2/3/4
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MS-7886 BOMList

Schematic Cfg	ERP NO	Remark	BOM
MS-7886/BEDGAMNGHLS			A
MS-7886/BEDAHRO			

 MSI <small>Micro Start International Co., Ltd.</small>	
COVER SHEET	
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[illegible]

Not supported HB on TYPE 1

Not supported HB on TYPE 1

M2 PCIe / SATA5 SATA6
Not supported PCIe on TYPE 0 1

M2 PCIe / SATA5 SATA6
Not supported PCIe on TYPE 0 1

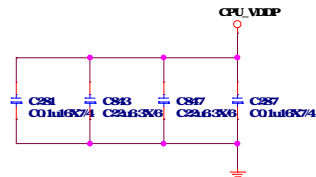
TYPE 0	PCIe	SATA
2	2	2
TYPE 2/3	2 or 4	2 or 0

Not supported GEX 4-15 on TYPE 1

PCIe1

Only supported on TYPE 2

Only supported on TYPE 2
Not supported GEX 8-15 on TYPE 0 3

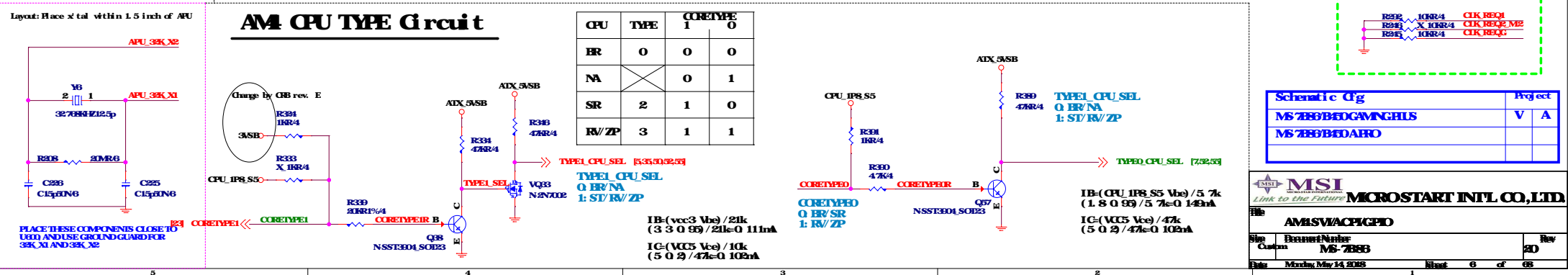
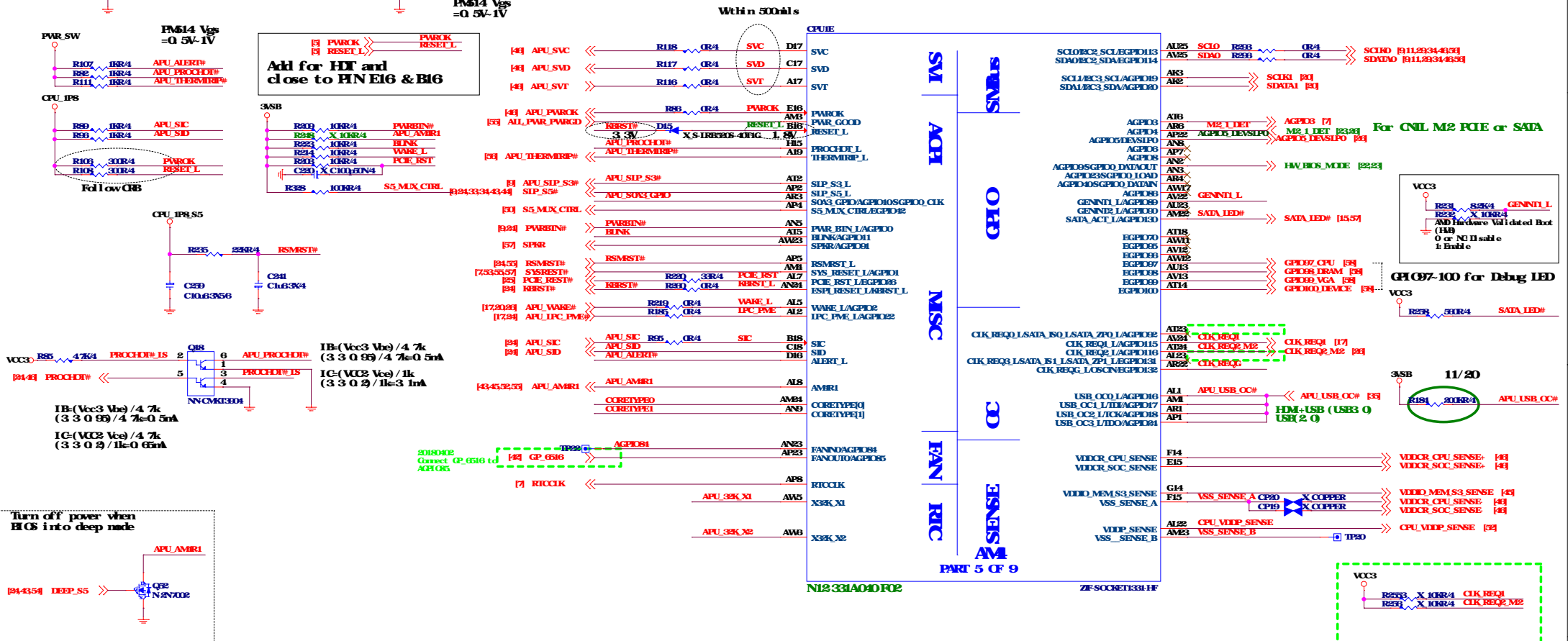


Within 1500 nls from APU
Within 1000 nls from APU

Within 1500 nls from APU
Within 1500 nls from APU
Within 1000 nls from APU

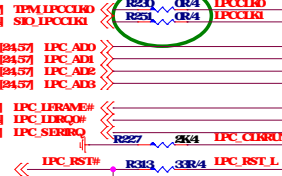
Schematic Qg	Project
MS 780BBDGAMNGHLS	V A
MS 780BBDAR0	

MSI MICROSTAR INT'L CO., LTD.	
AMPCESATAE	
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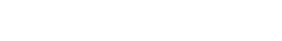
Follow G8



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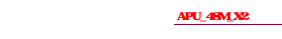
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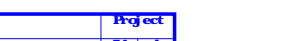
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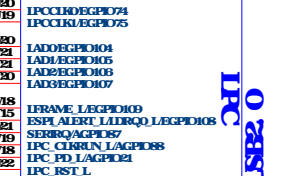
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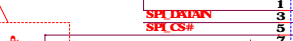
38/20



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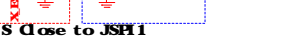
40/20



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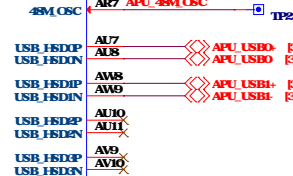
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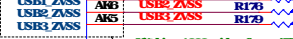
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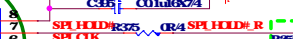
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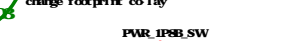
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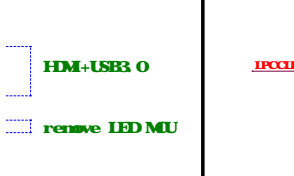
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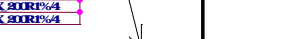
65/20



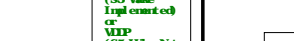
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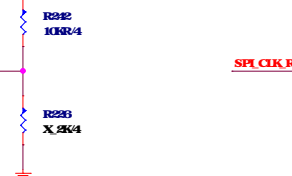
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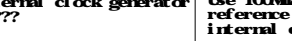
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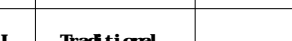
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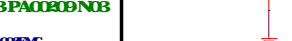
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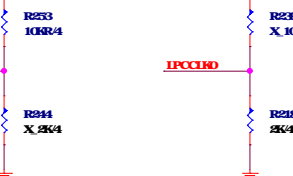
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1. 5V@ 25A



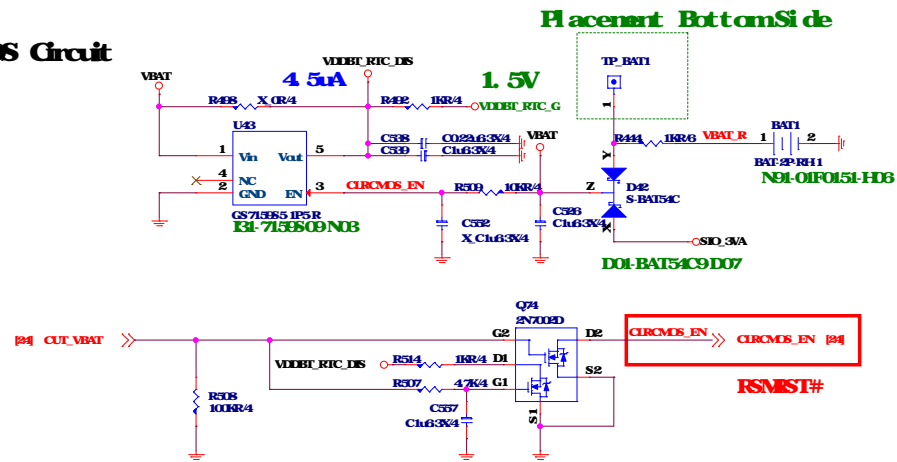
DDP 8 5A



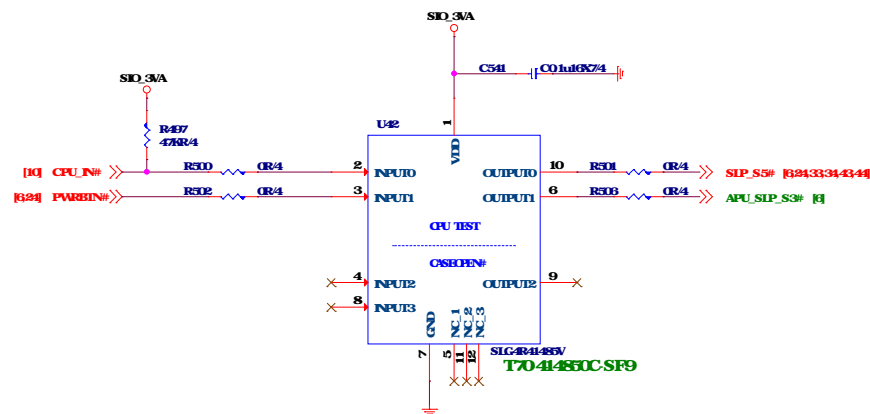
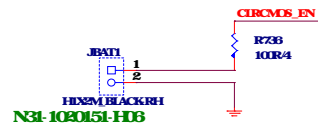
ZF-SOCKET1331-HF **N12 331A040 F02**

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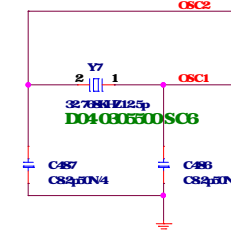
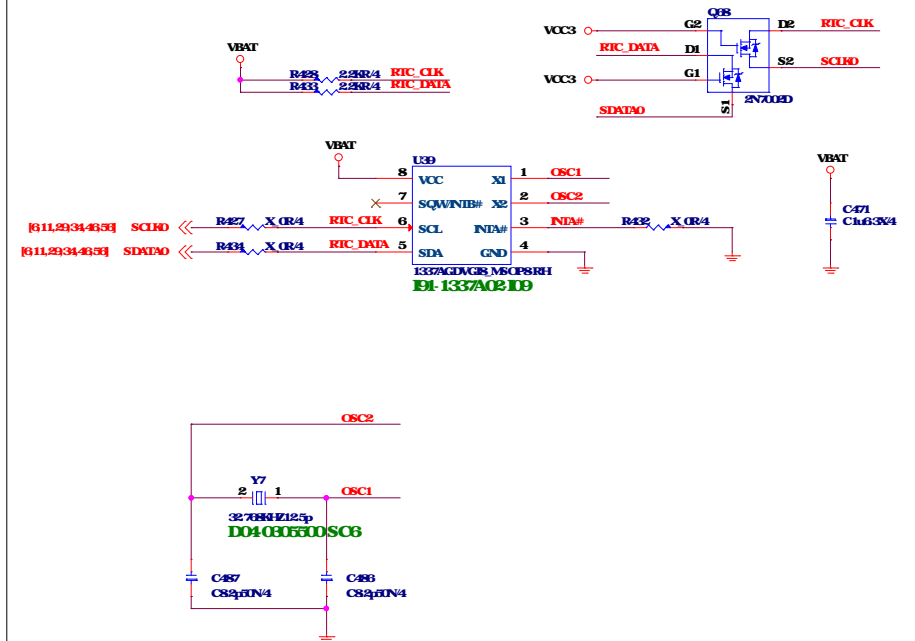
RTC & Clear CMOS Circuit



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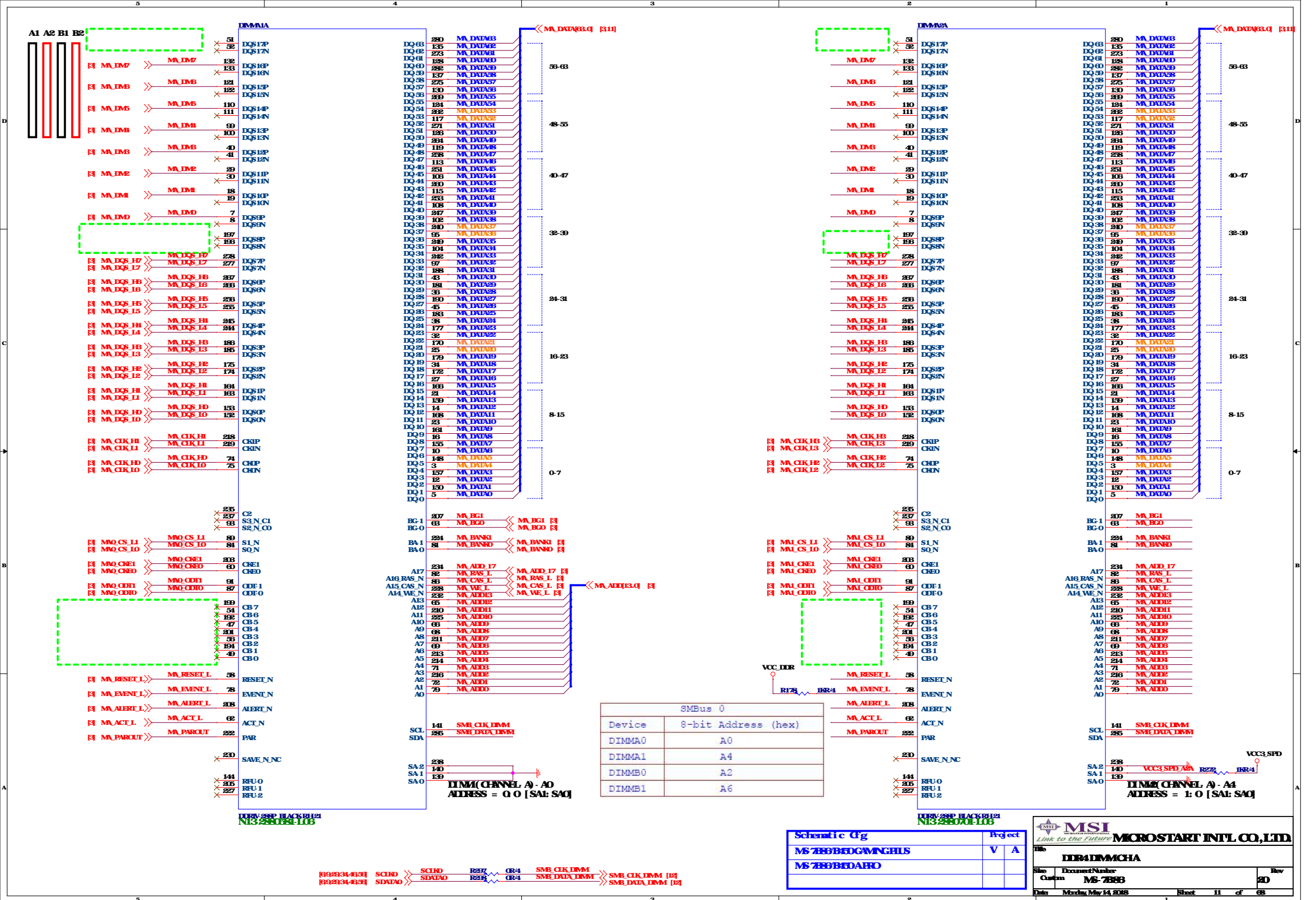


RTC Backup

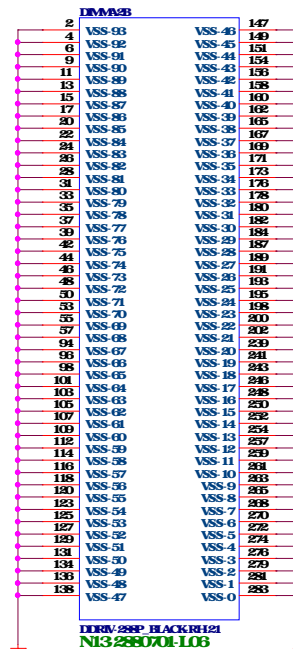
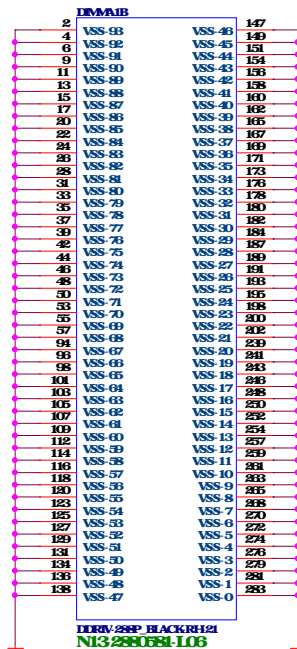
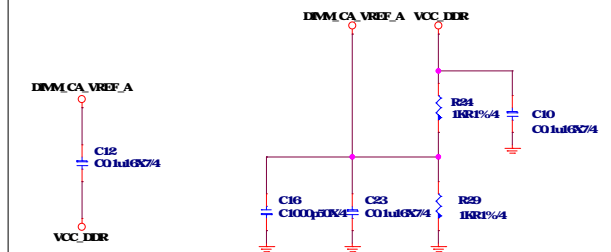
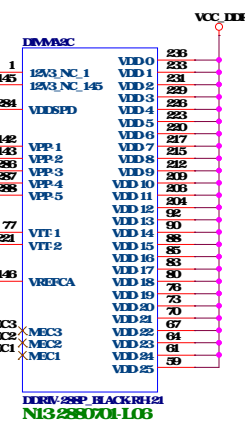
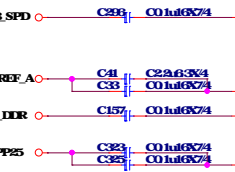
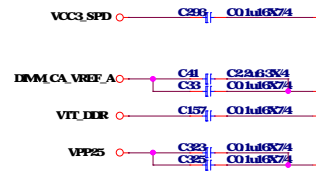


GND

AM
PART 9 CF 9

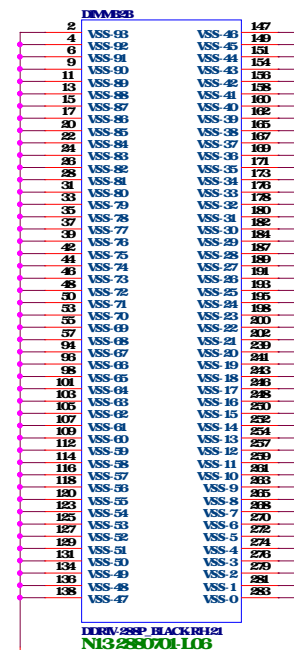
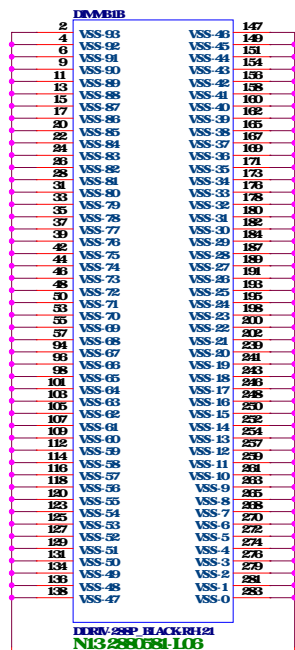
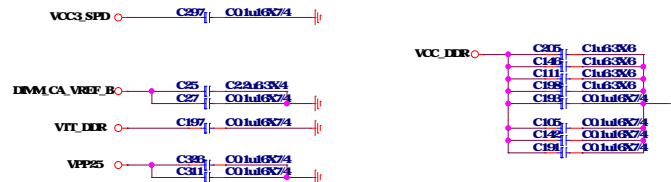
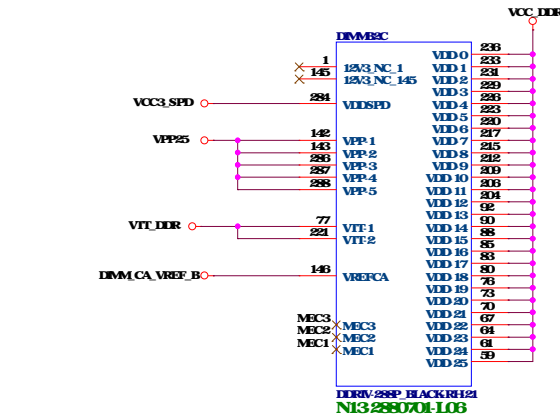
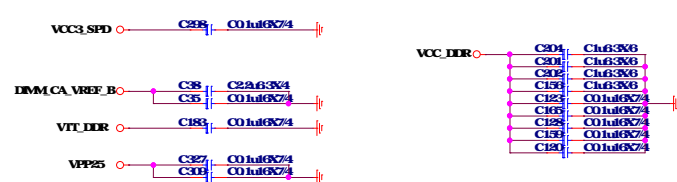
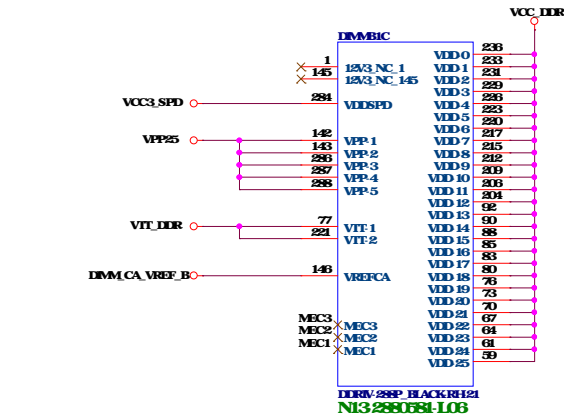
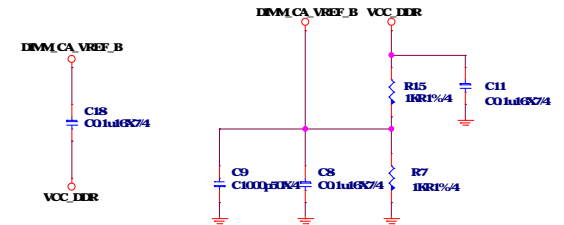


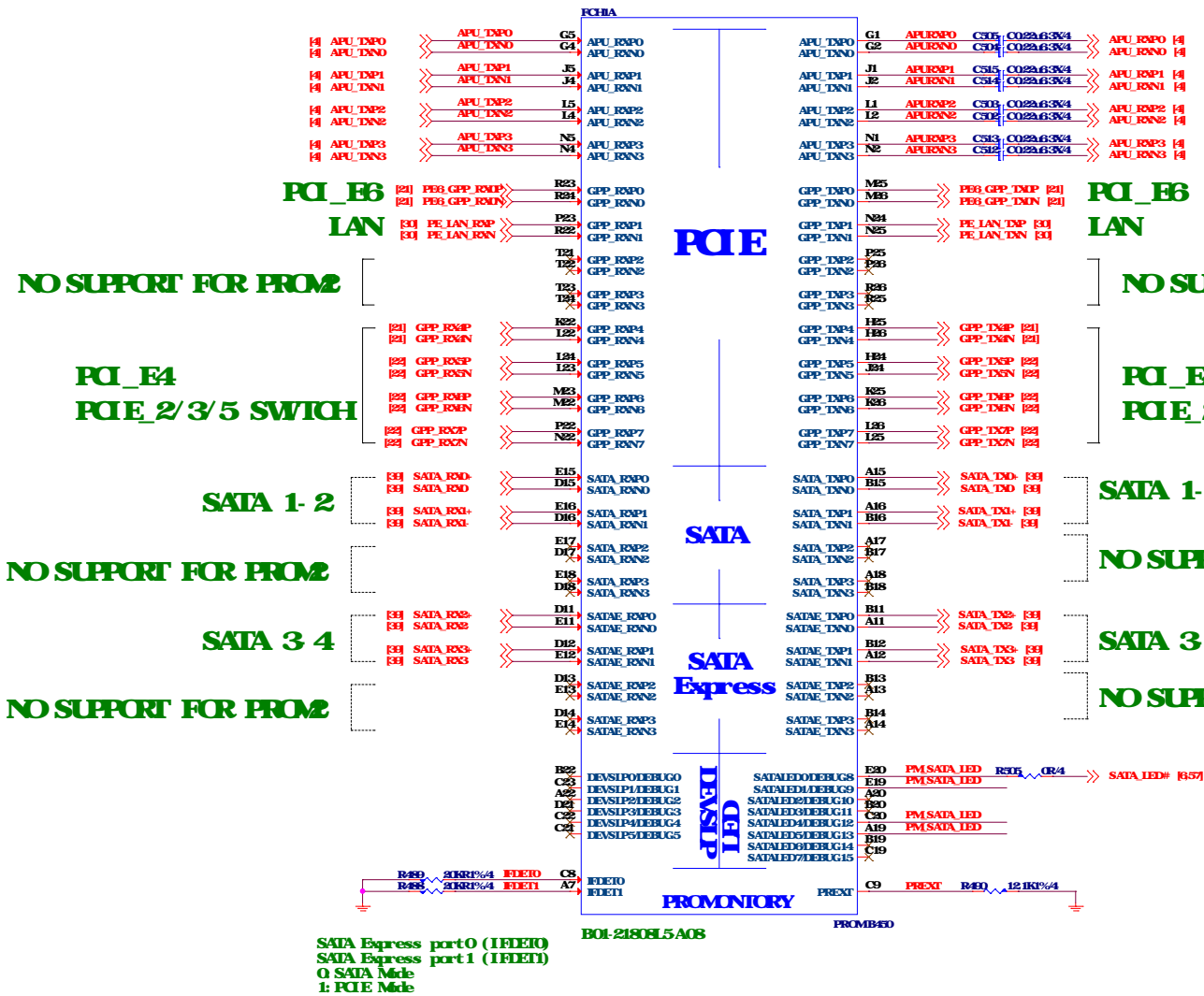
F10
VCC3 1 2 VCC3_SPD
F-SPR P280T
D080B01000P16



DDR VREF

(place resistors close to DIMM)





Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0	USB_HSD Port0~5	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1	CLK0~1
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2,3不能用
CLK1-3不能用

Appendix D USB Port to OC Pin Mapping


USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1.3不能用

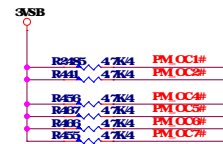
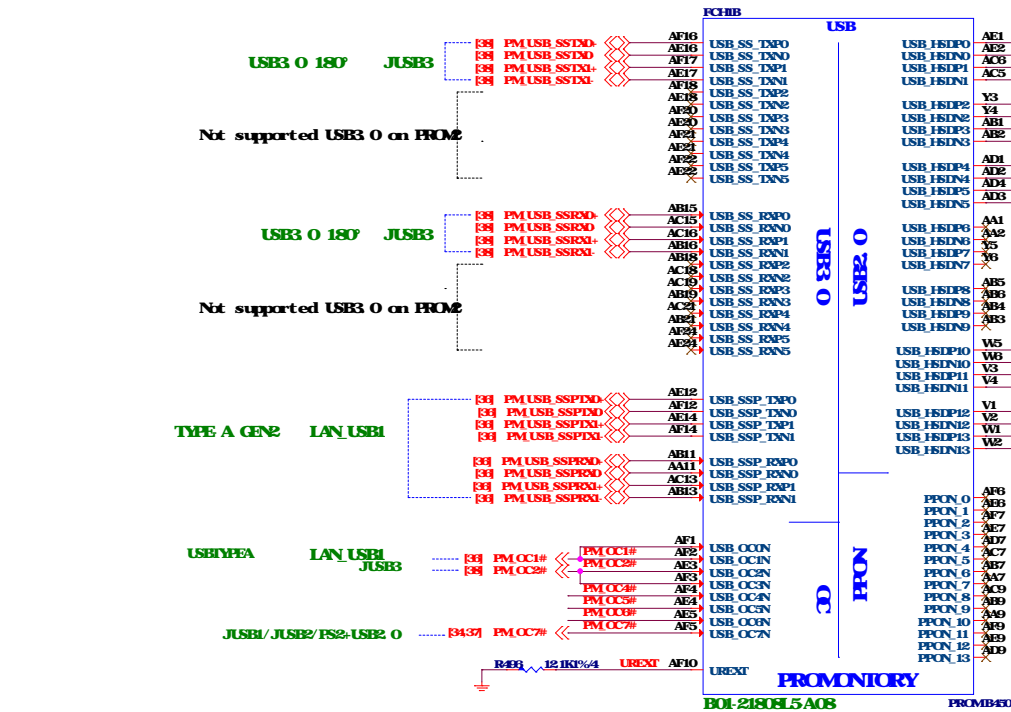


Link to the Future

MICROSTAR INT'L CO., LTD.

Promontory-USB/OC

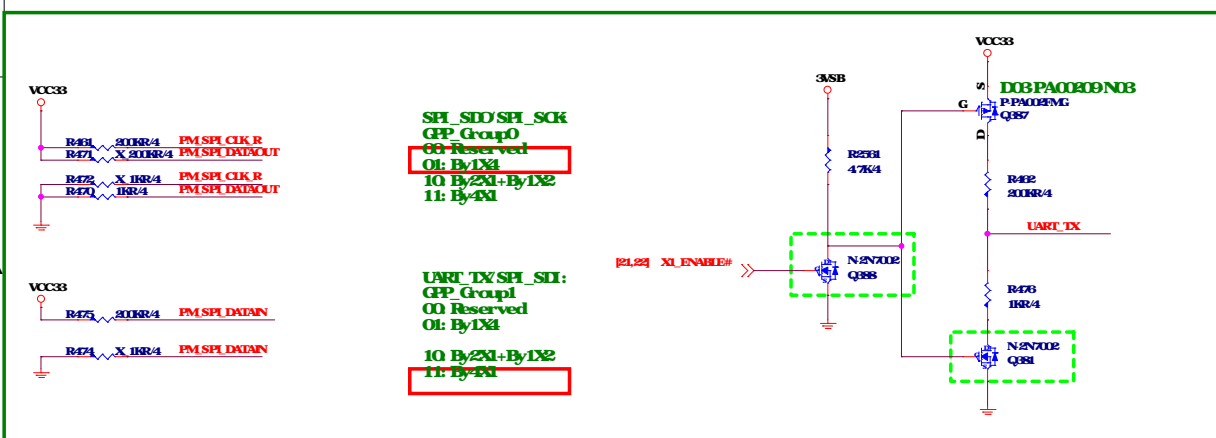
Site	Document Number	Rev
Custom	MS-7383	2.0
Date	March, May 14, 2015	Sheet 10 of 68



The schematic diagram illustrates the PMIC (Power Management Integrated Circuit) and its connections. The PMIC is shown as a central component with various pins and internal components like capacitors and resistors. Key connections include:


- Power and Ground:** VCC3 is connected to the PMIC. Ground connections are shown at the bottom.
- Resistors:** R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038

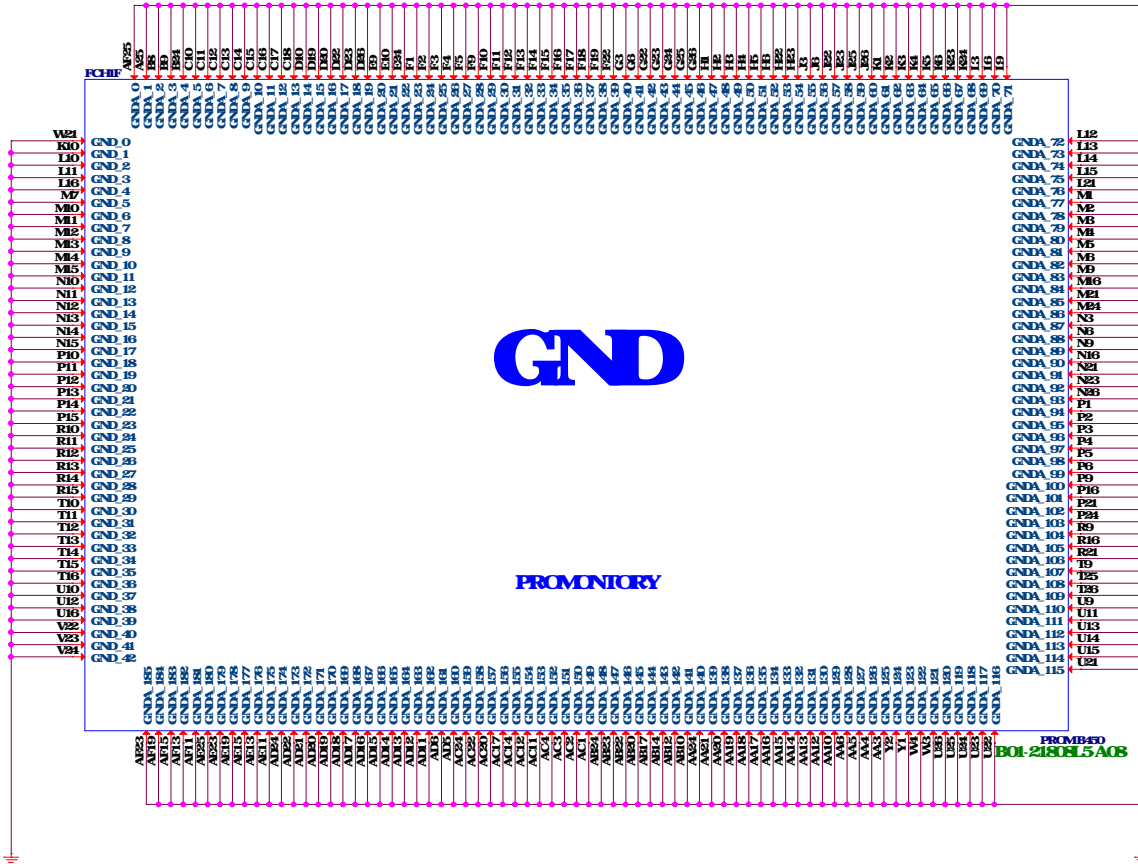
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-5	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SSP Port0 USB_SSP Port1	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0

[illegible]

The diagram illustrates the connection between the B450 Gaming Pro and B450 Gaming Plus motherboards. The B450 Gaming Pro (top) has a VCC3 pin connected to three pins on the B450 Gaming Plus (bottom): M1D1, M1D2, and M1D3. The B450 Gaming Pro is labeled 'B450 GAMING Pro 601-7386' and the B450 Gaming Plus is labeled 'B450 GAMING PLUS 601-7386'.

	M1D1	M1D2	M1D3
B450 GAMING Pro 601-7386	1	0	0
B450 GAMING PLUS 601-7386	0	0	0
	1	1	0

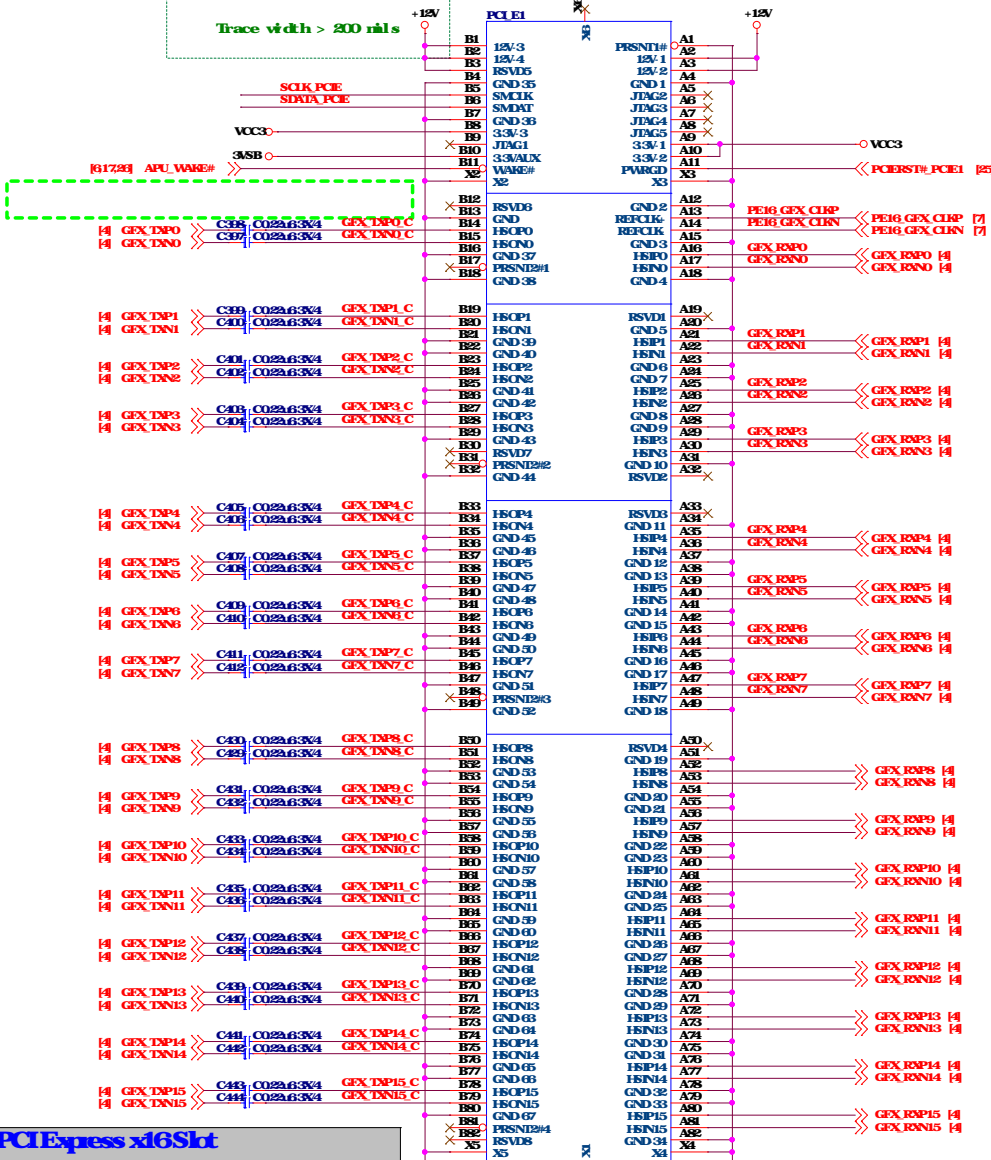
 MSI <small>Computer Communications</small> <i>Link to the Future</i>		MICROSTART INT'L CO., LTD.	
Promotory CLK/ACPI/GPD			
Sale Customer	Discount/Order MS-7888	Rev 2D	
Date	Monday, May 14, 2006	Sheet	17 of 68



PCI EXPRESS x16 Slt

PCI E1

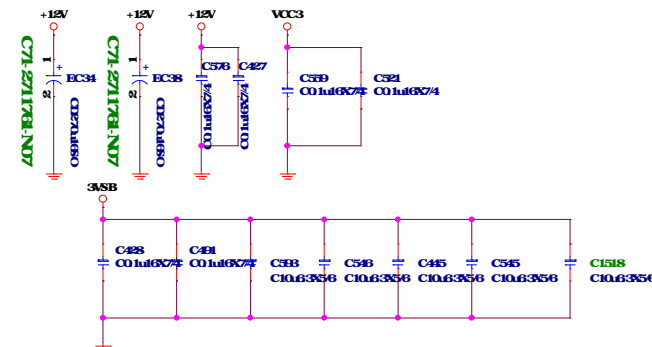
Trace width > 200 mils



PCI Express x16 Slt			
+12V	-	55A	
+VCC3	-	3A	
+3V3_S5	(wake)	-	375mA
+3V3_S5	(nowake)	-	20mA

CLK_PCE [R35] X (R4) CLK_PCE [R21]
DATA_PCE [R37] X (R4) DATA_PCE [R21]

CLK_PCE [R35] X (R4) CLK_PCE [R21]
DATA_PCE [R37] X (R4) DATA_PCE [R21]



PCI Express x8 Slt			
+12V	-	55A	
+VCC3	-	3A	
+3V3_S5	(wake)	-	375mA
+3V3_S5	(nowake)	-	20mA

MSI
Link to the future
MICROSTART INT'L CO., LTD.

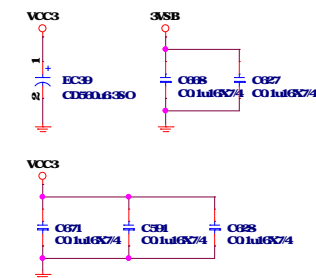
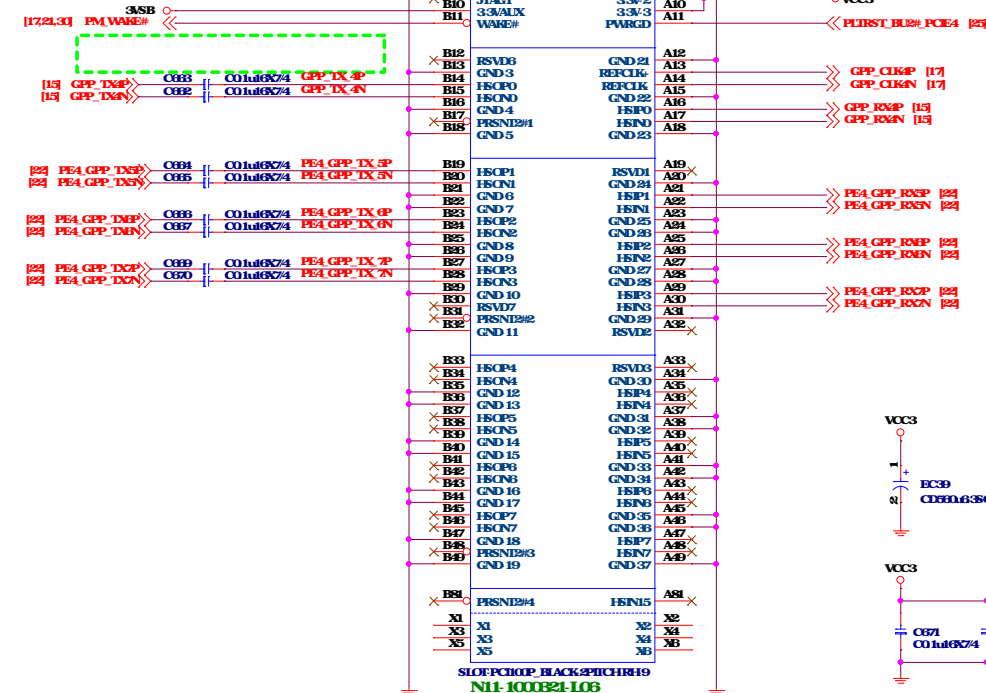
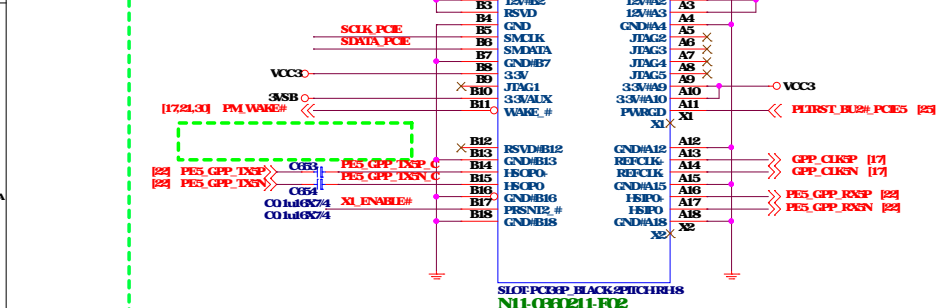
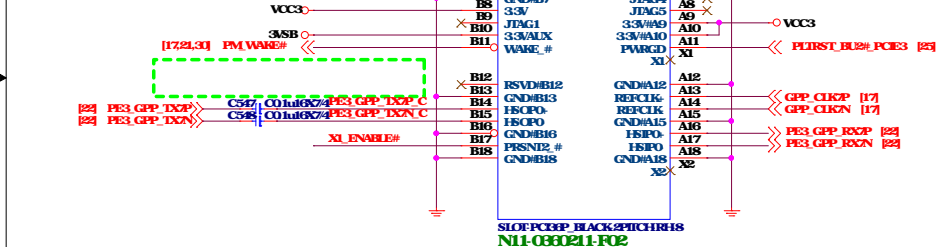
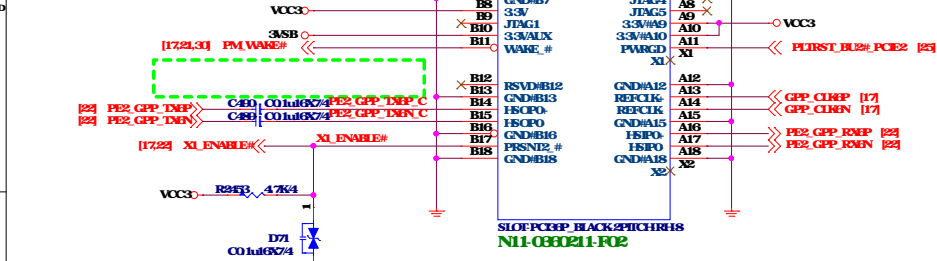
PCI E1/E4 X16/S8

Doc No: MS-7888

Date: Mar 14, 2008

Sheet: 20 of 68

PCI E2



PCIExpress x4Slot*1		
+12V		- 21A
+VCC3		- 3A
+3V3_S5	(vale)	- 375mA
+3V3_S5	(novale)	- 20mA
PCIExpress x1 Slot*4		
+12V		- 2A
+VCC3		- 12A
+3V3_S5	(vale)	- 1500mA
+3V3_S5	(novale)	- 80mA

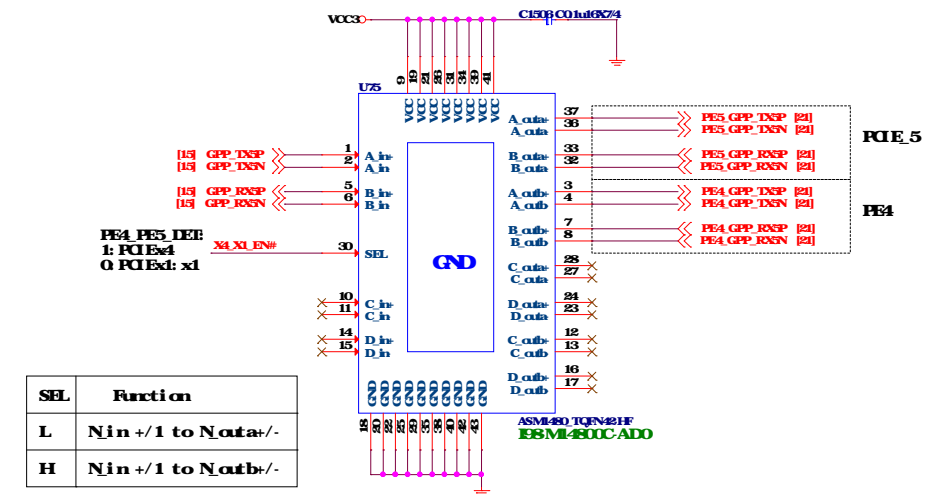
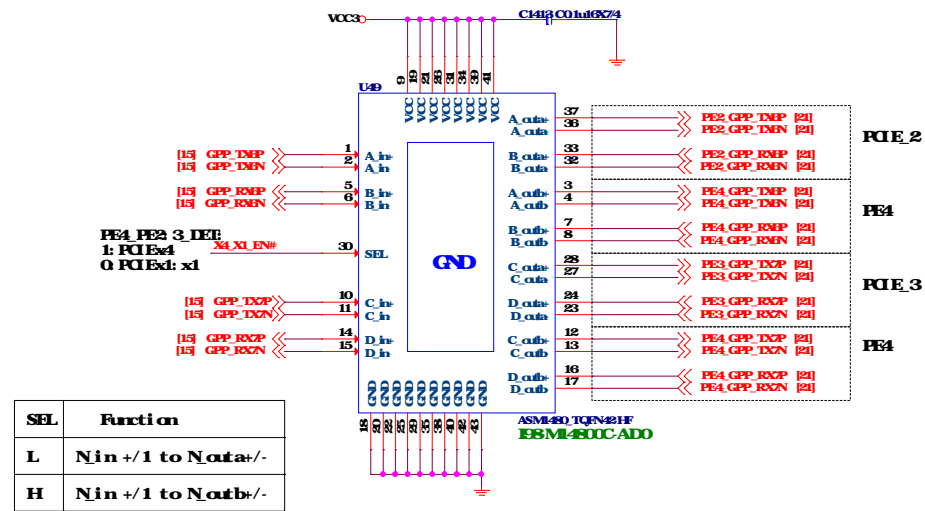
 **MSI**
MICROSTAR INTERNATIONAL
Link to the Future **MICROSTART INTL CO., LTD.**

PCI E2 E3 E5/E4 X1/X4

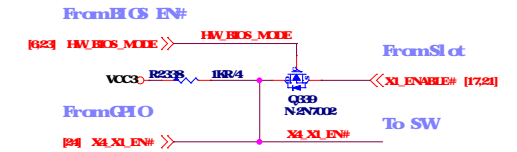
File	Document Number	Rev
Custom	MS-7B96	20

Date: Monday, May 14, 2018 Sheet: 21 of 68

PCI_E4 and PCIe_2 / 3 / 5 Switch



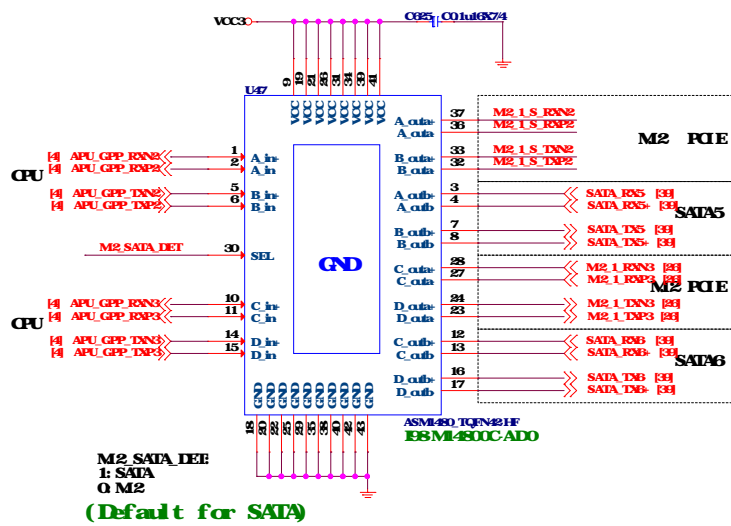
PCIe Lanes control circuit



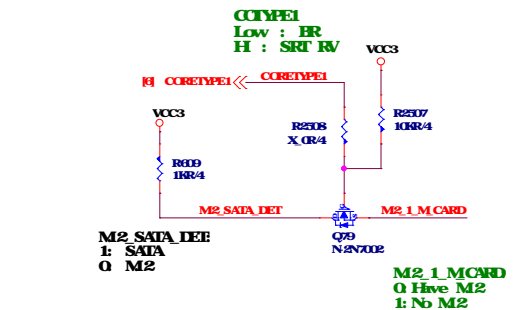
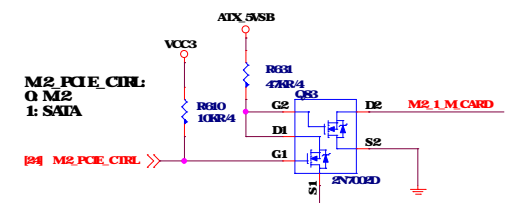
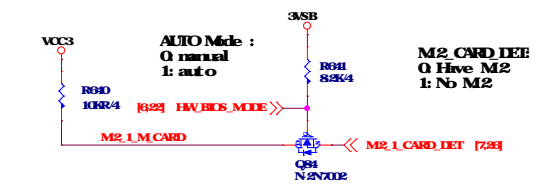
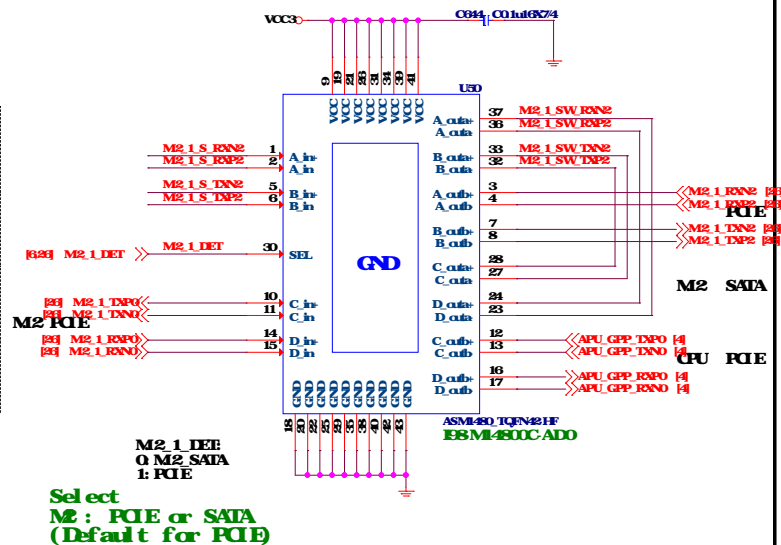
UART_TX/SPI_SDI:
GPP_Group1
00: Reserved
01: By1X1
10: By2X1+By1X2
11: By4X1 (def)


	HIGH_CFG_MIDE	Q39	Q81	XL_ENABLE#	FMSH_DRAIN
Minimal x4	L	OFF	OFF	X	11: By4cd (def)
Minimal x1, x1, x1, x1	L	OFF	OFF	L	10: By1cd
HW x4	H	ON	ON	H	11: By4cd (def)
HW x1, x1, x1, x1	H	ON	ON	L (Stuff PCIe 1)	10: By1cd

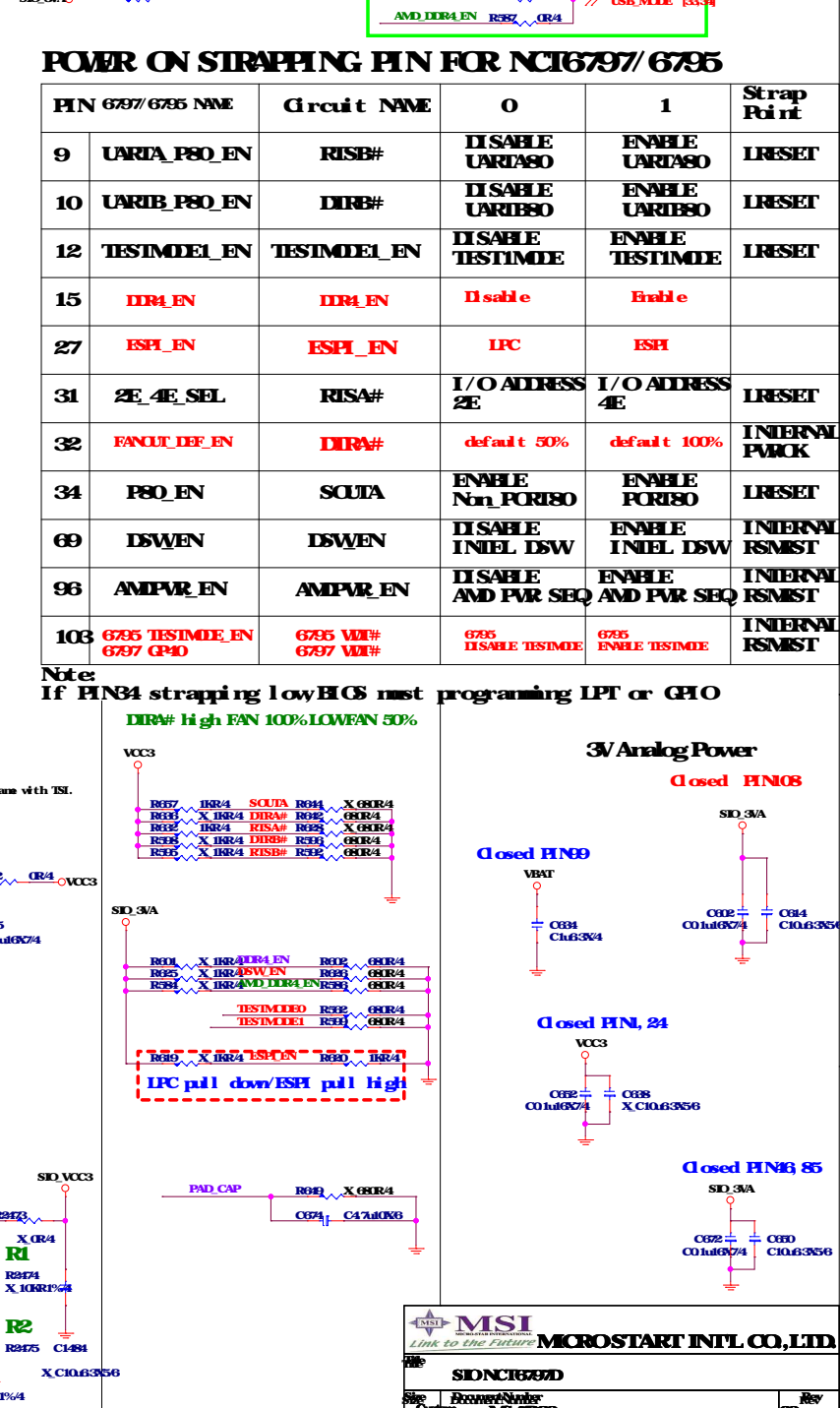
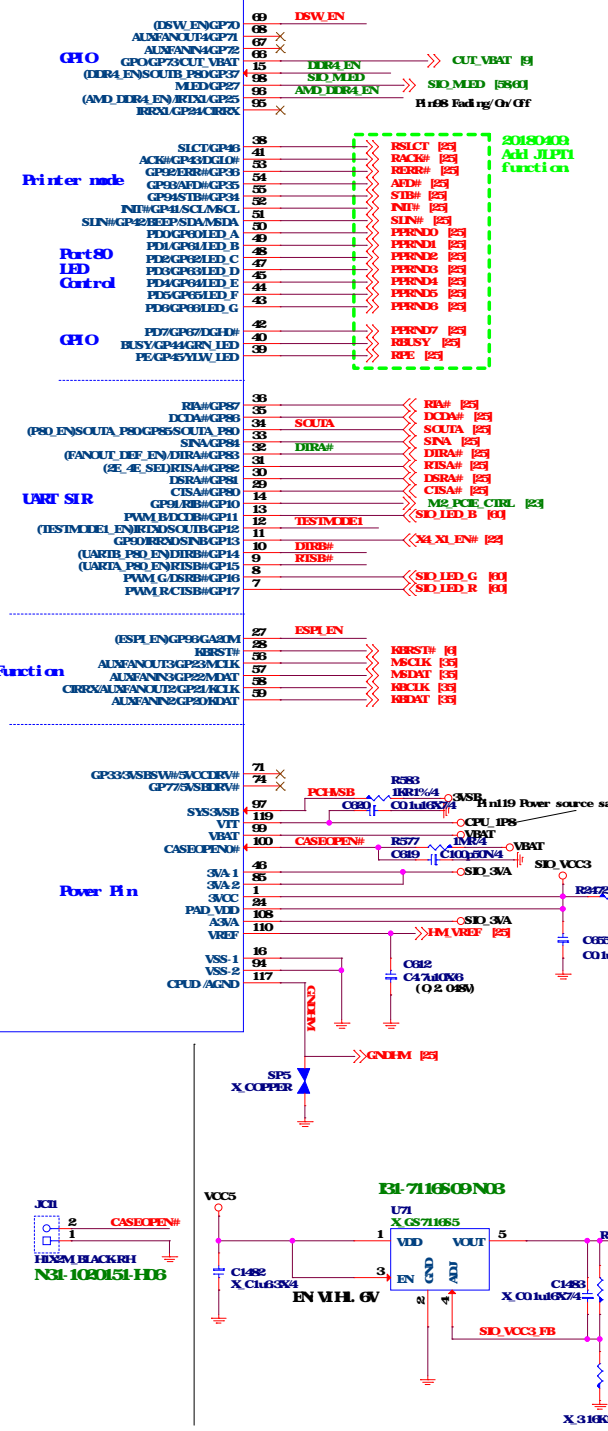
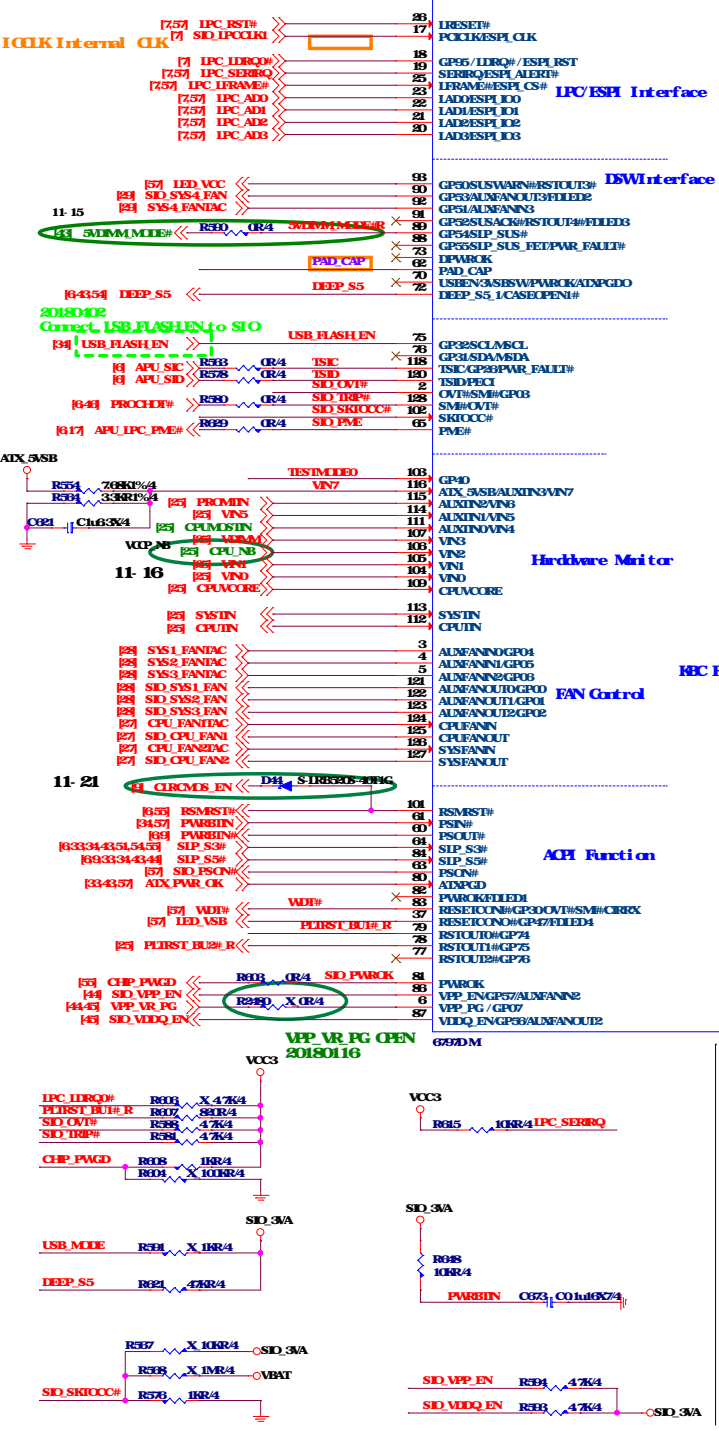
M2_1 and SATA5 6 Switch



SEL	Function
L	N _{in} +/1 to N _{outa} +/-
H	N _{in} +/1 to N _{outb} +/-



CPU	TYPE	CORETYPE	
		1	0
IR	0	0	0
NA		0	1
SR	2	1	0
R/ZP	3	1	1



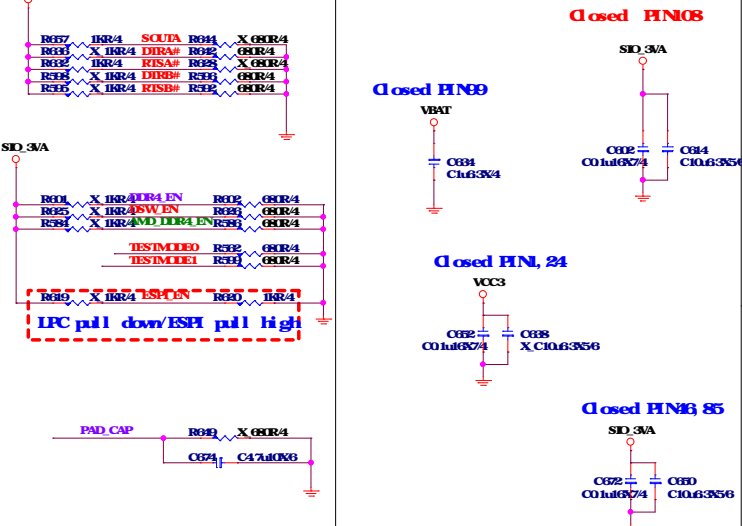
POWER ON STRAPPING PIN FOR NCI6797/ 6795

PIN 6797/ 6795 NAME		Circuit NAME	0	1	Strap Point
9	UARI_A_P80_EN	RISE#	DISABLE UARI_A80	ENABLE UARI_A80	LRESET
10	UARI_B_P80_EN	DIRB#	DISABLE UARI_B80	ENABLE UARI_B80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE	ENABLE TESTMODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ISH_EN	ISH_EN	IPC	ISH	
31	2E_4E_SEL	RISA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DIRA#	default 50%	default 100%	INTERNAL PMICK
34	P80_EN	SCUTA	ENABLE Non_POR180	ENABLE POR180	LRESET
69	DSWEN	DSWEN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMIST
96	AMPVR_EN	AMPVR_EN	DISABLE AND PVR SEQ	ENABLE AND PVR SEQ	INTERNAL RSMIST
103	6795 TESTMODE_EN 6797 GP40	6795 VOUT# 6797 VOUT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMIST

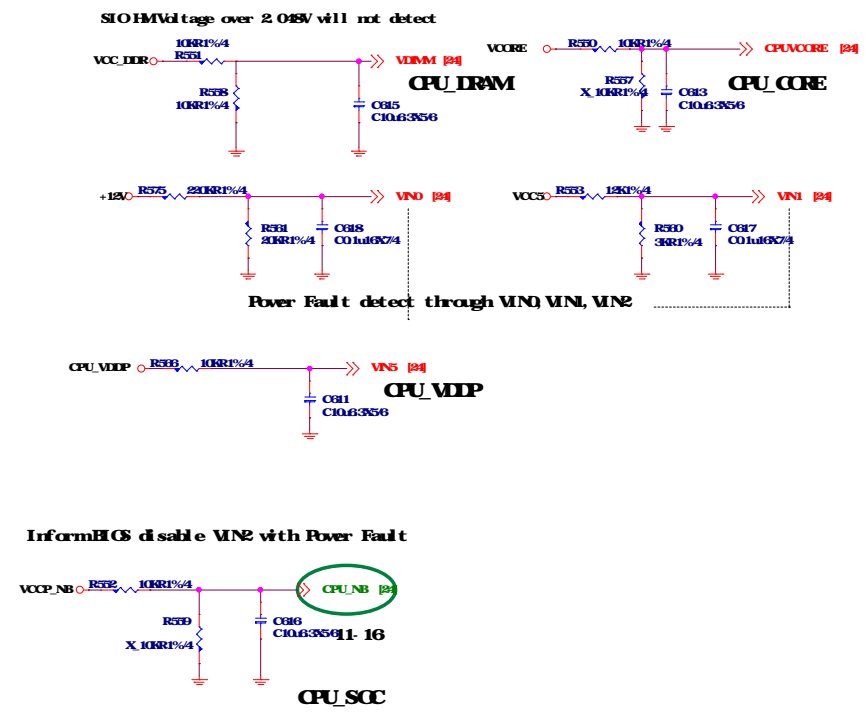
Note: If PIN34 strapping low HCS must programming IPT or GPIO

DIR# high FAN 100%LOWFAN 50%

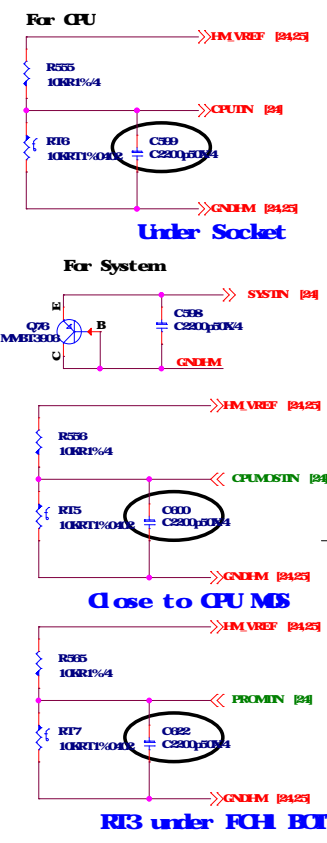
3V Analog Power



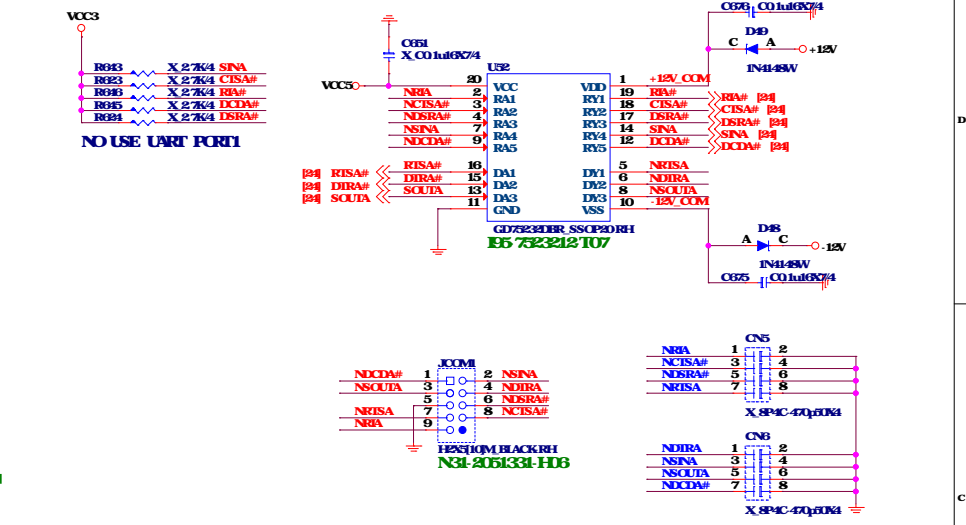
HW Monitor - Voltage



TEMP SENSOR

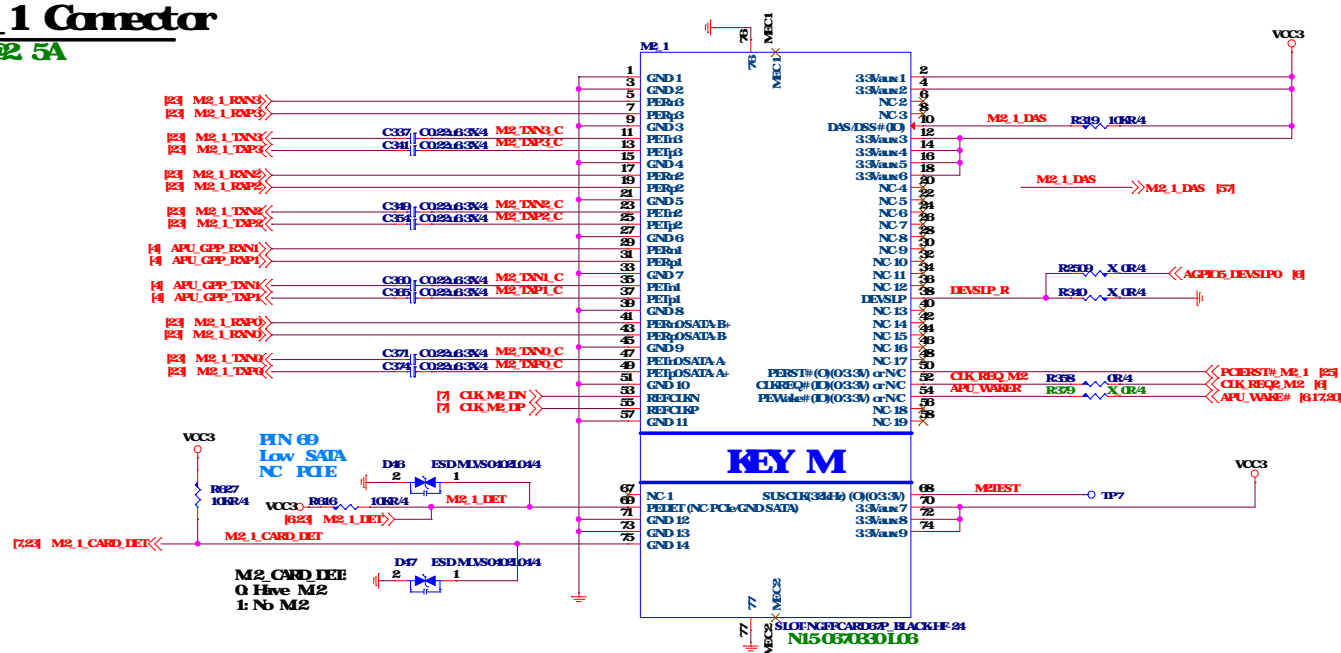


COMPORT

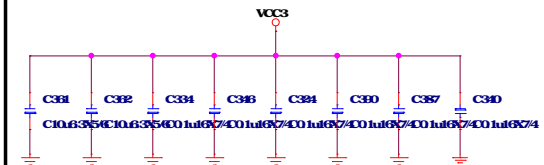


M2_1 Connector

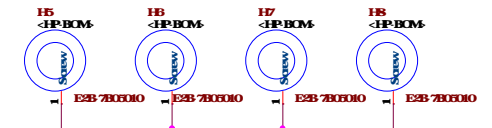
3 3V@ 5A



3 3V@ 5A



E2B 78010A89 E23 1203514A89



Footprint: H240D173, H240D173
E2B 78010A89 E23 1203514A89
E2B 78010A89 E23 1203514A89

Schematic Cg		Project	
M2_1	MS 78010A89	V	A
M2_1	MS 78010A89		

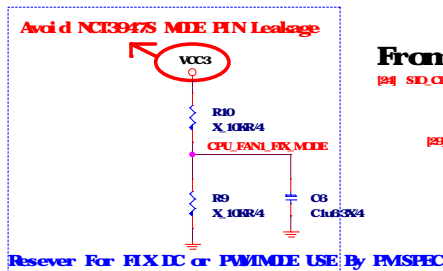
MSI MICROSTART INT'L CO., LTD.	
M2_1	
Rev	Rev
Rev	Rev
Date	Date
Rev	Rev

TYPE L : 4 PIN CPU FAN USE NC13947S USE PCH GPIO CONTROL FAN MDE

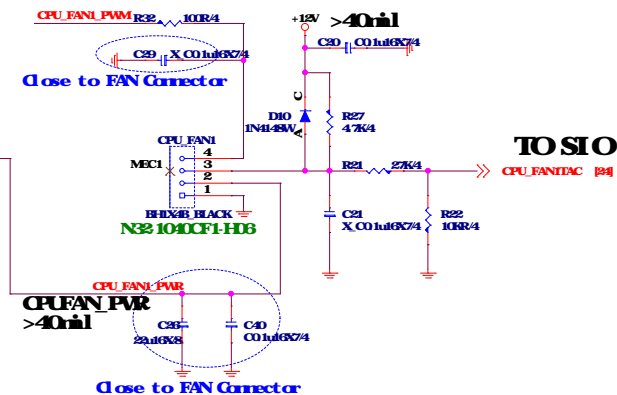
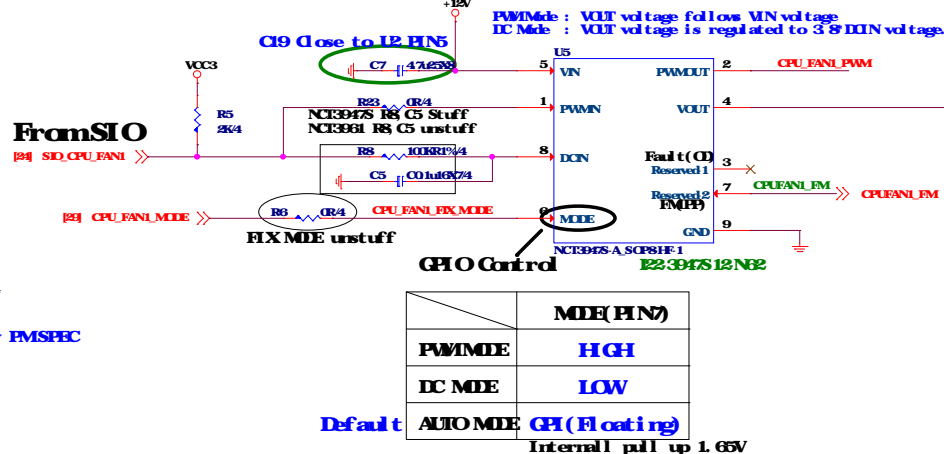
20180120
CPU FAN - Type L
Pump FAN - Type K

1. Mode GPIO BIOS can switch PWM/DC MDE
2. FMBIOS can read FAN PWM/DC MDE

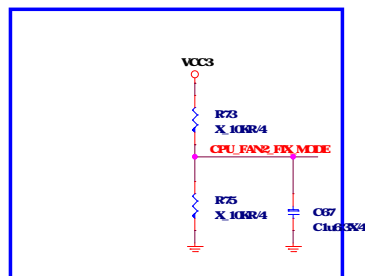
CPU_FAN1



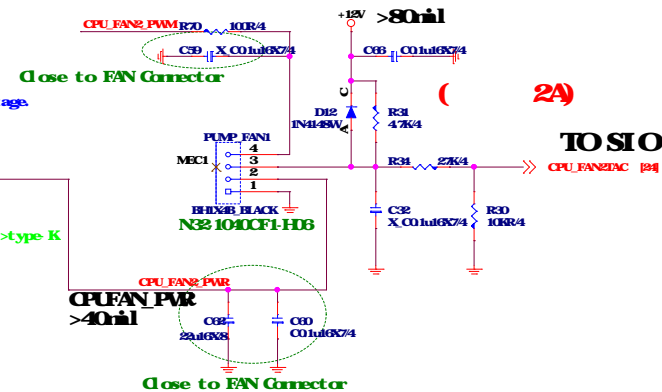
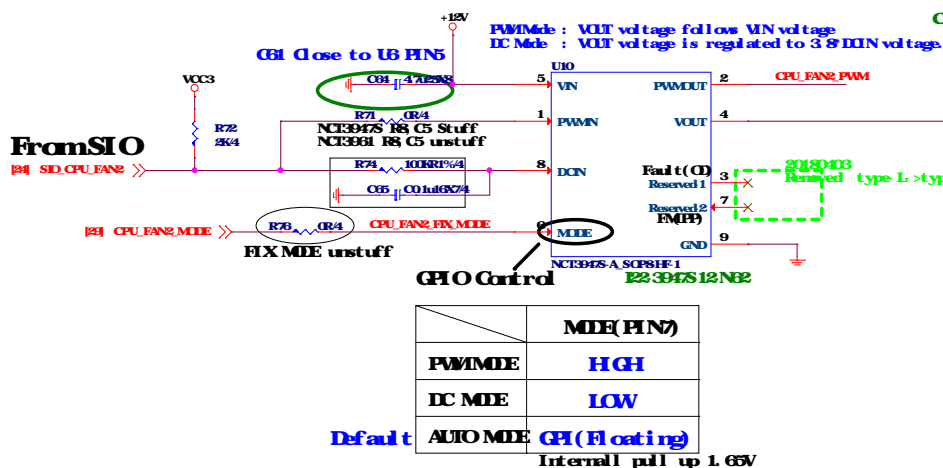
If C19 place high thermal area, You can change X2R cap



PUMP_FAN1



If C61 place high thermal area, You can change X2R cap



If C291 place high thermal area, You can change XTR cap
C291 Close to U24 HU

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8VDCIN voltage



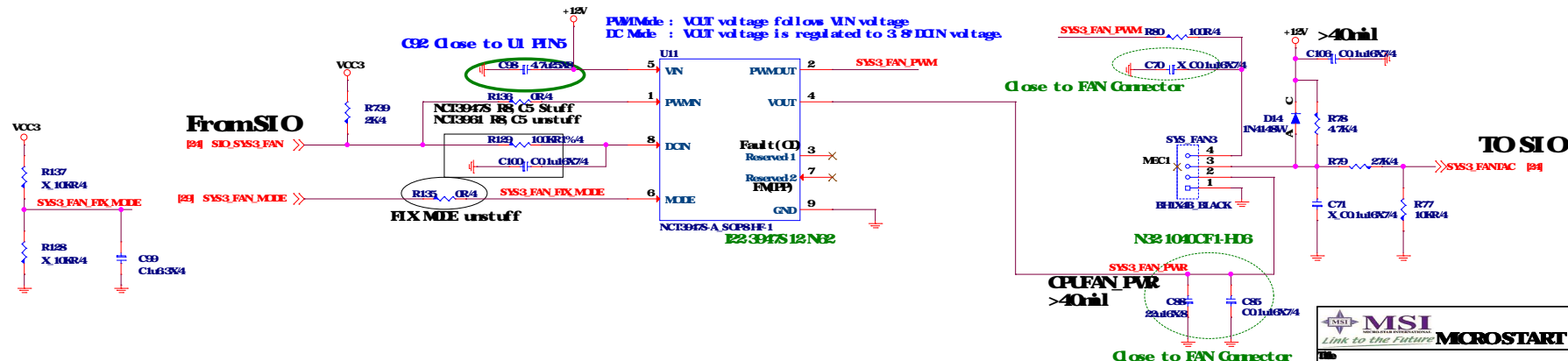
C651 Close to U58 PIN5

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8VDCIN voltage



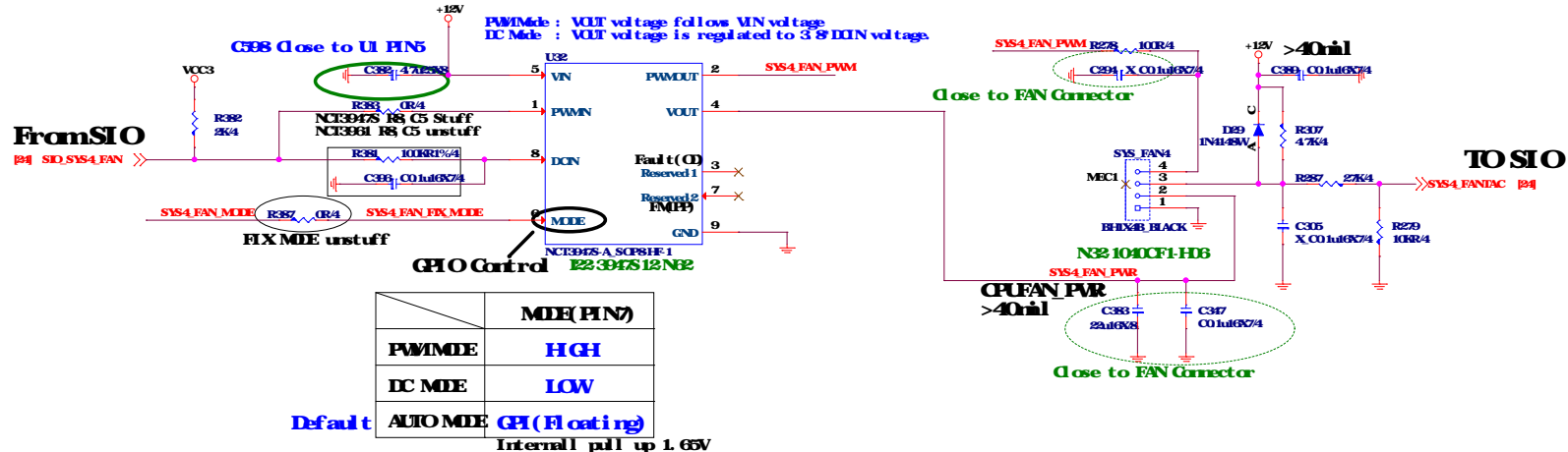
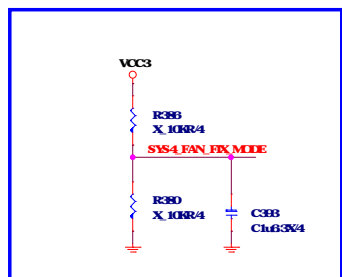
C92 Close to UI HN5

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8VDCIN voltage.



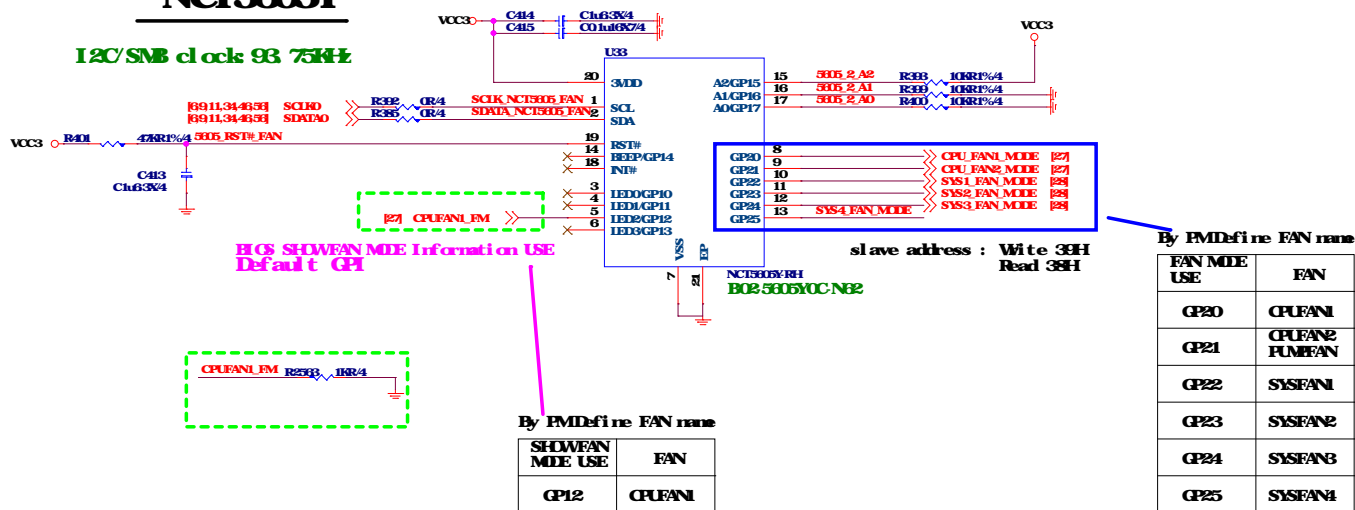
TYPE K: 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area, You can change X7R cap



NCT5605Y

I2C/SMB clock: 93.75kHz



1. GENERAL DESCRIPTION

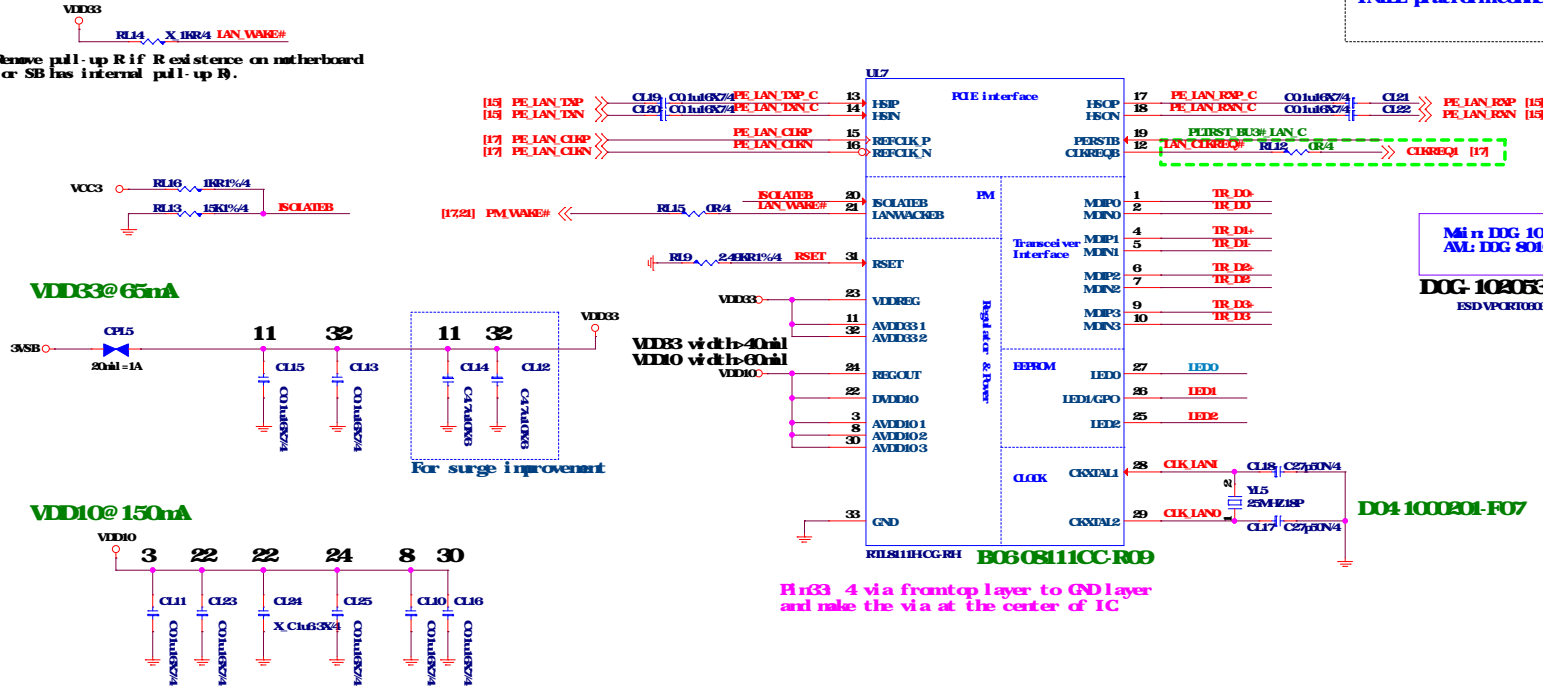
The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W
---	---	---	---	----	----	----	-----

RIL811H Giga LAN

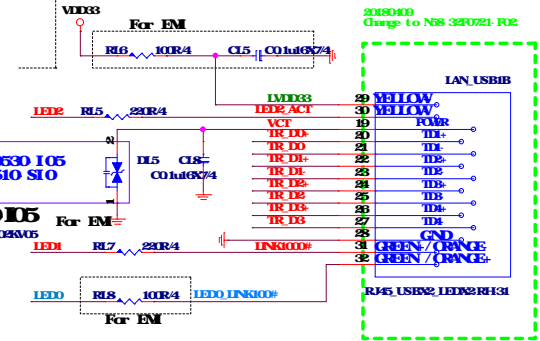
Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



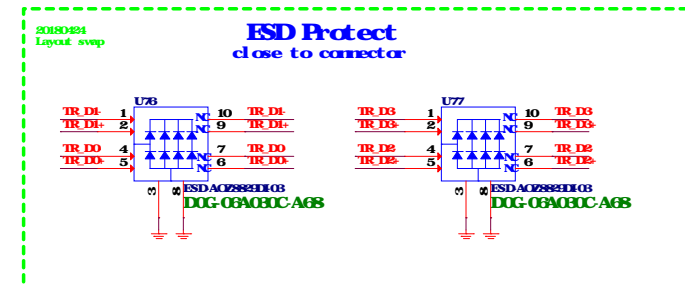
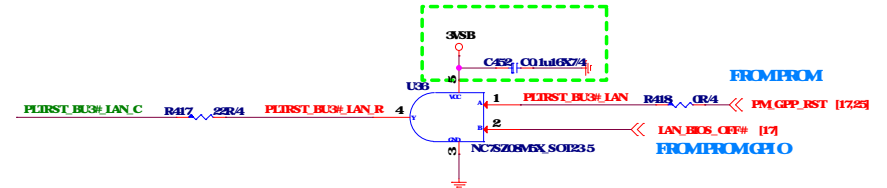
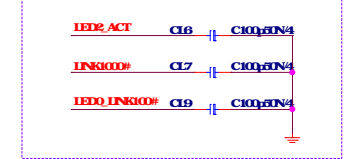
Pin33 4 via fronttop layer to GND layer
and make the via at the center of IC

Pin19
AND platform connect to PCIe_RST#
don't connect to A_RST#
INIEL platform connect to FLT_RST#

LAN Connector



For EM



811H POWER Consumption

	3.3V @ mA	mW
10 Mbit/s/100M	9.9/84.69	32.67/279.48
100 Mbit/s/100M	48.11/92.44	158.79/305.05
Giga 100M/100M	124.5/177.57	410.85/585.98
ALPS	5.50	18.15

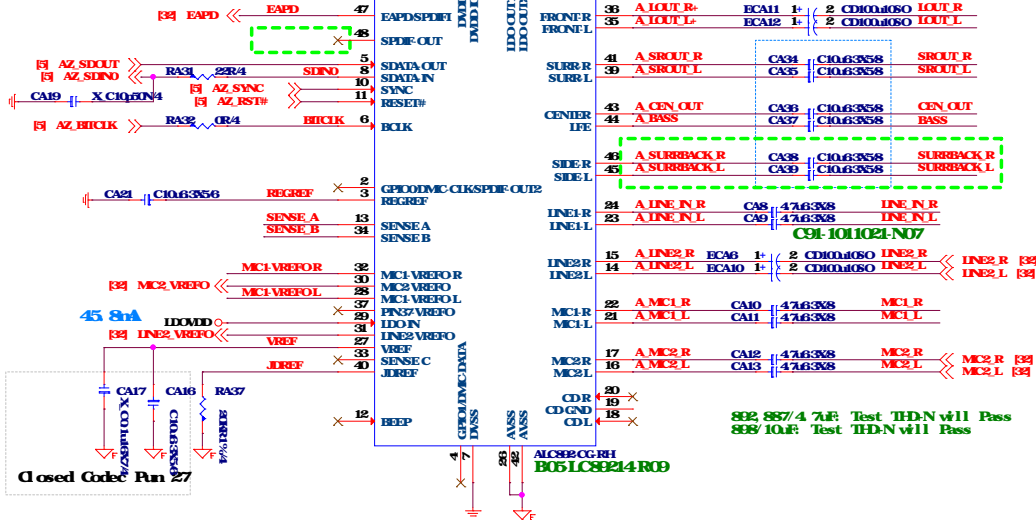
ALC892

Follow APU power well

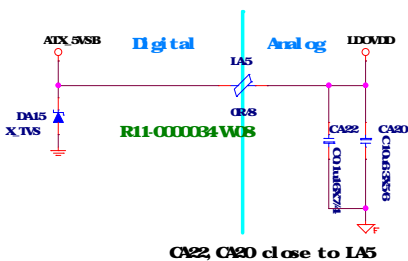
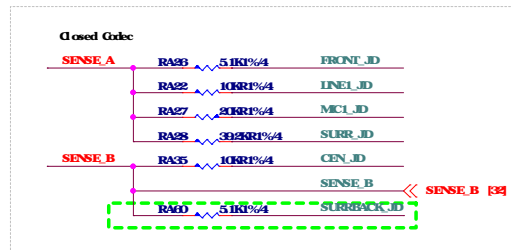
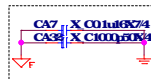
11mA

Closed Codec

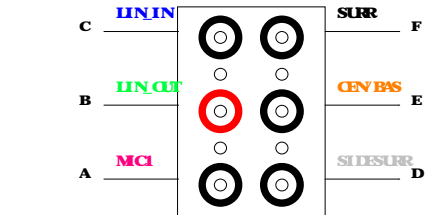
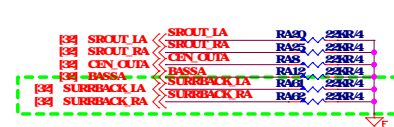
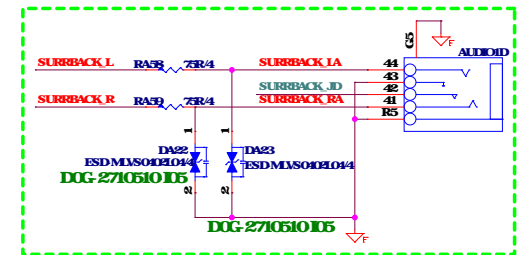
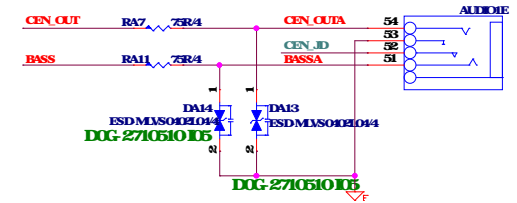
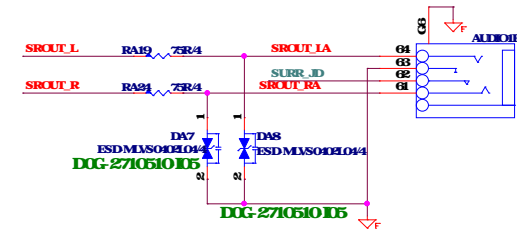
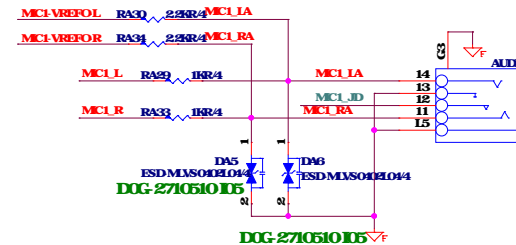
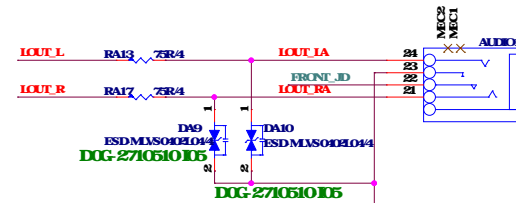
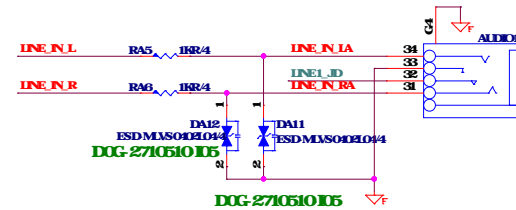
VOC3

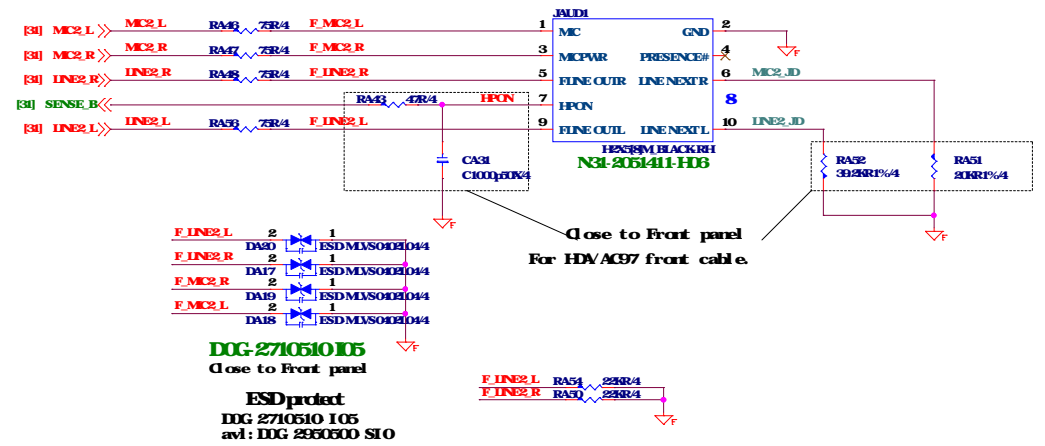
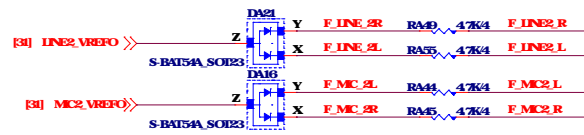


EVI

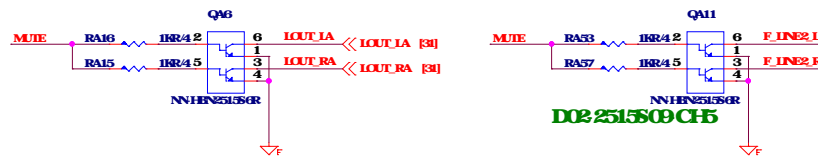
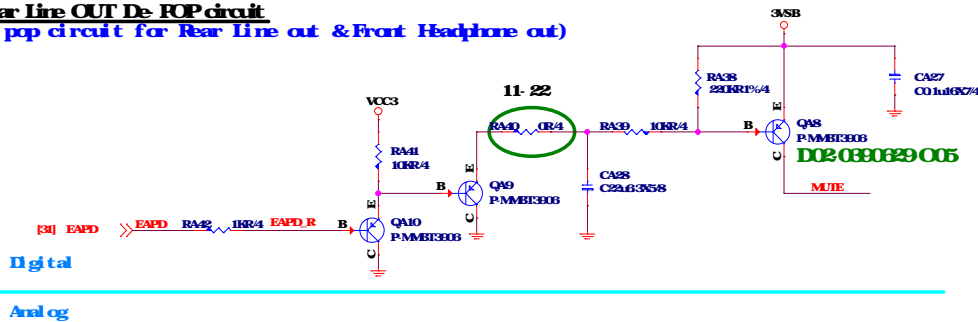


CA22, CA20 close to LA5

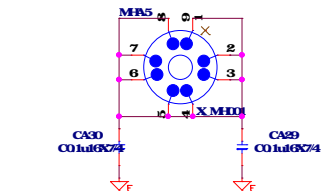
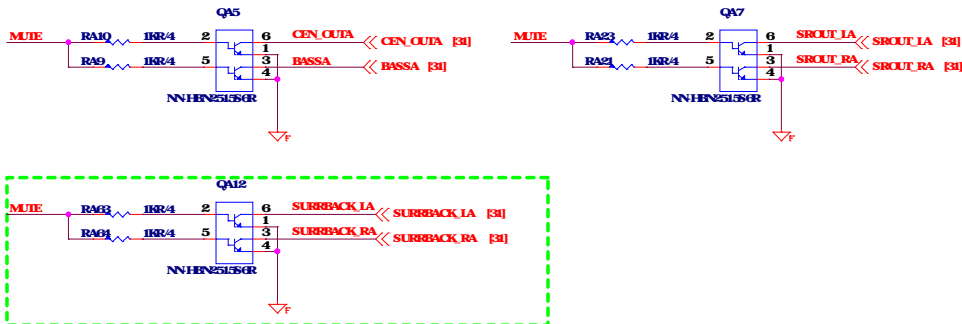




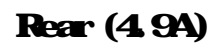
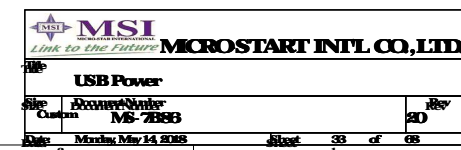
Rear Line OUT De POP circuit (De pop circuit for Rear Line out & Front Headphone out)



(add de pop circuit by FMspec or customer request,
NOTE: add de pop circuit need to change CA5, CA6, CA7, CA9 to TVS)



8 7A

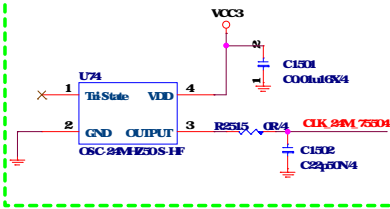
**Front (3 8A)**

USB Flash BIOS

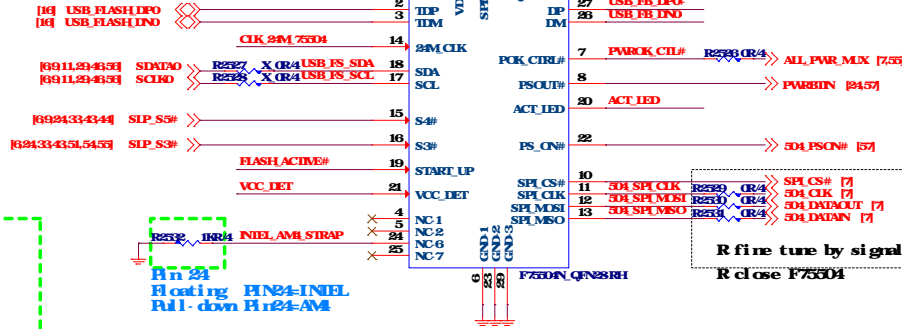
F75504 layout placement must meet to spi/usb trace length spec with host.
As far as possible place near to host.

CLK running in S0 don't require in sleep

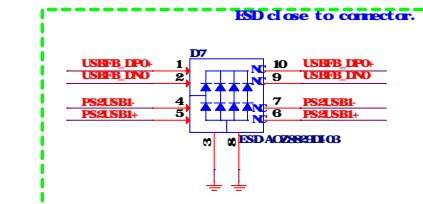
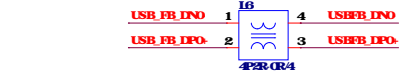
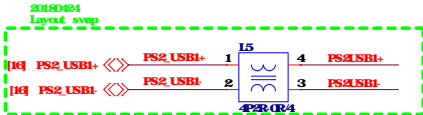
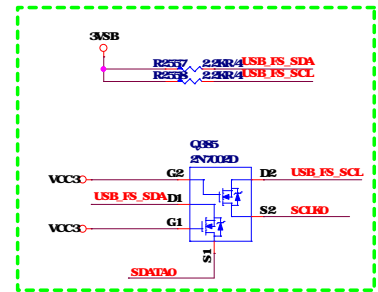
20180402
Add 2MHz crystal.



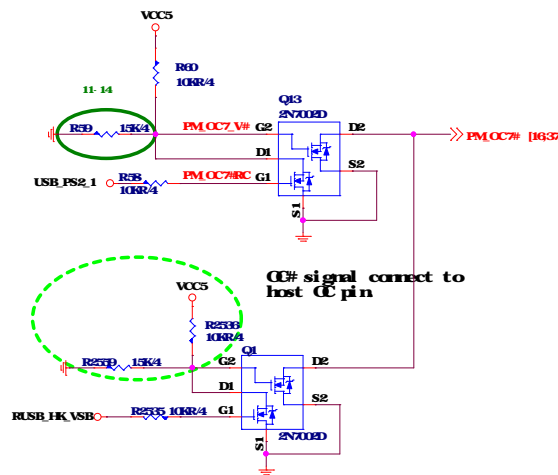
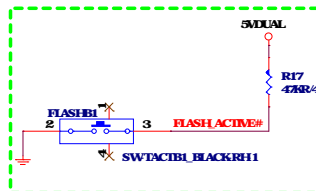
Host USB connector



Pin 24
Floating INTEL
Pull-down R124=1M

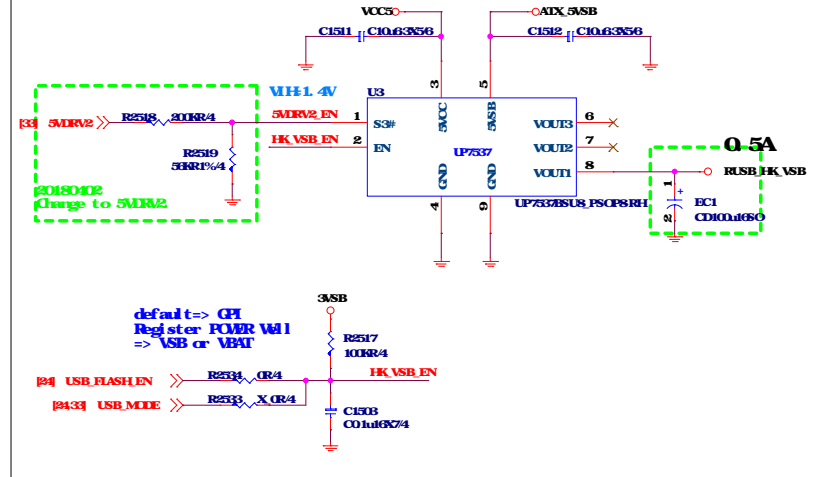


20180402
Follow module circuit, use usb3.0 ESD
for good eye diagram
20180424
Layout swap



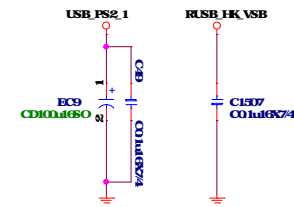
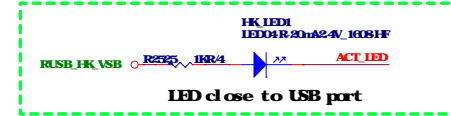
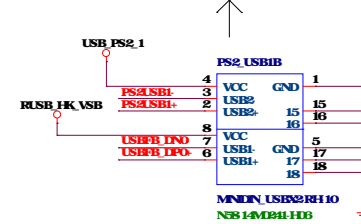
CC# signal connect to host CC pin

HUKEY POWER

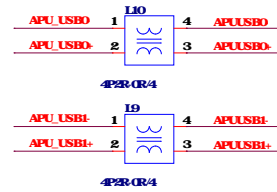
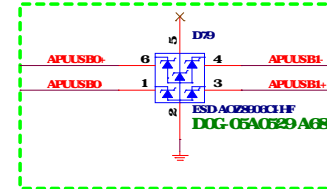
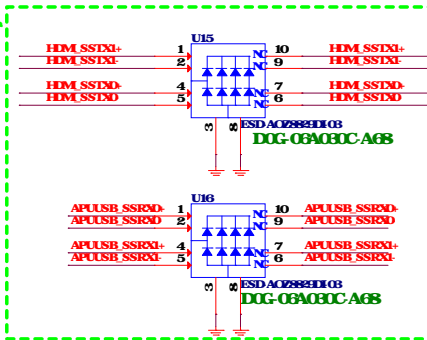


default t=> GPI
Register POWER W11
=> USB or VBAT

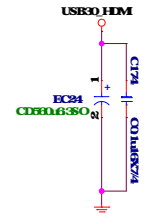
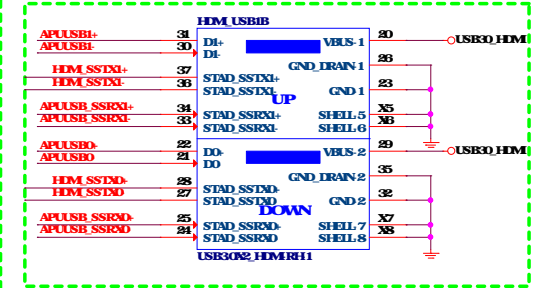
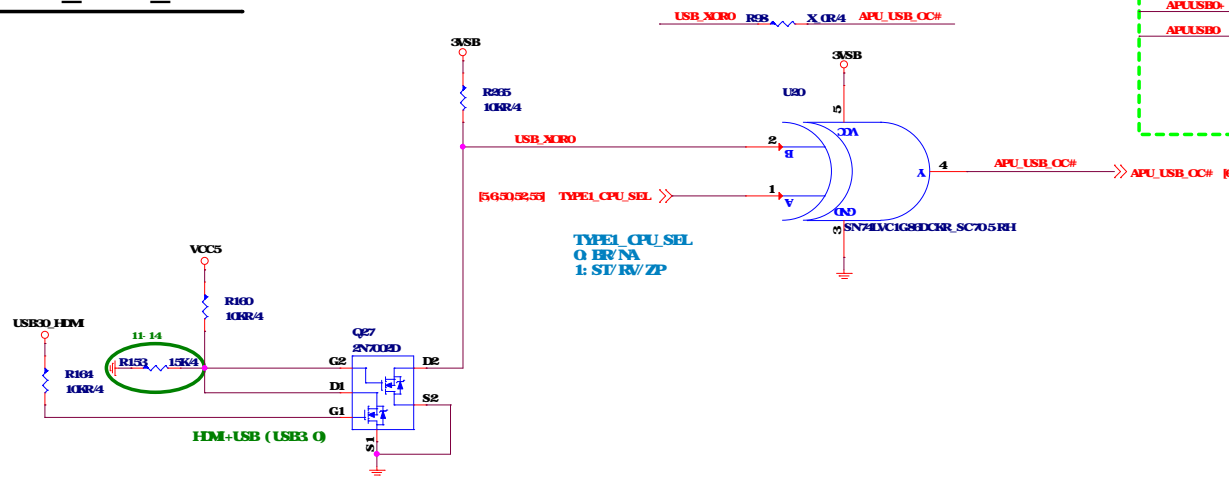
USB Connector power come from UP7537
provide (USB Hub Connector same)



5V@1A

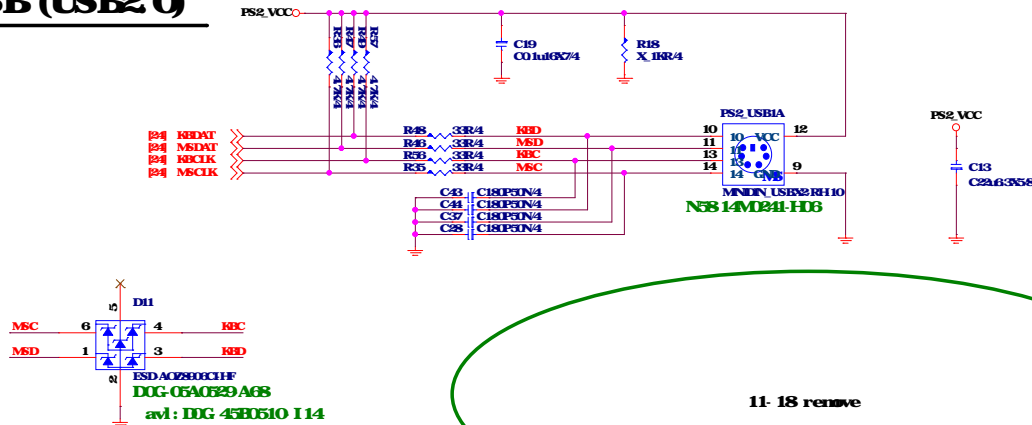
20180436
layout: swap


20180409
Connector change to N58 37M0121-106

**APU_USB_OC**

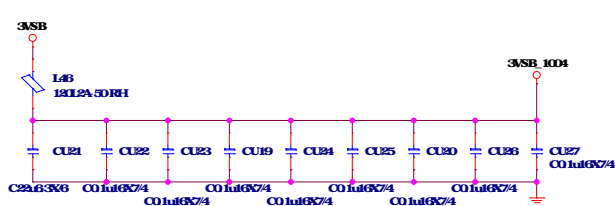
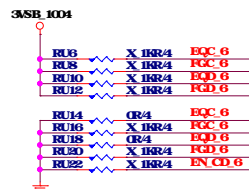
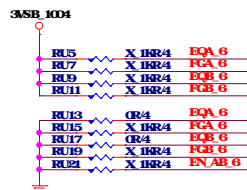
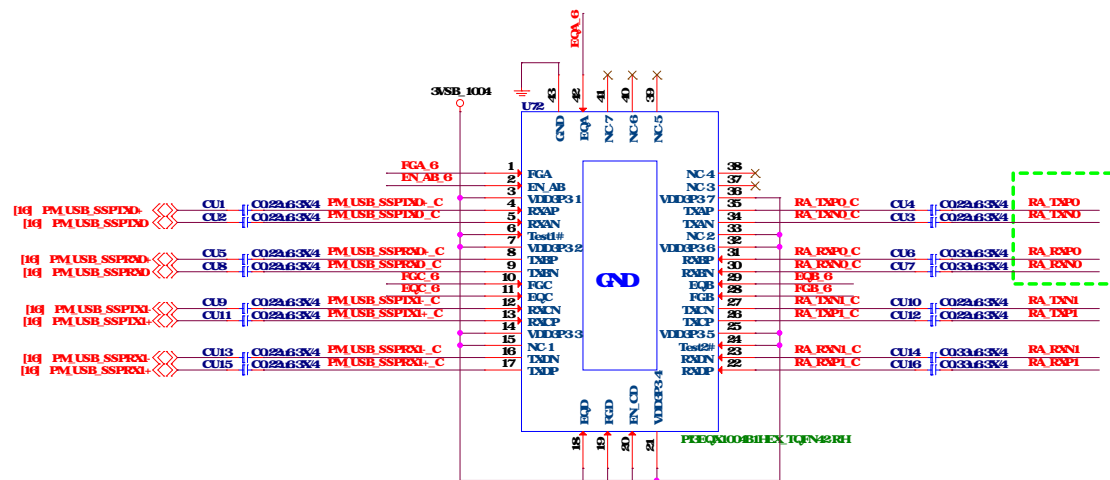
	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

PS2+USB (USB2 0)

5V@1A

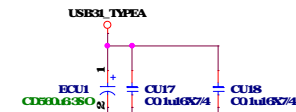
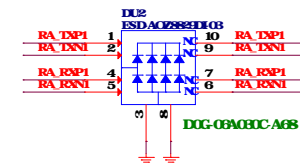
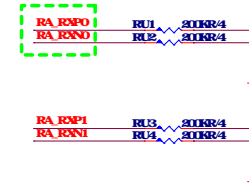
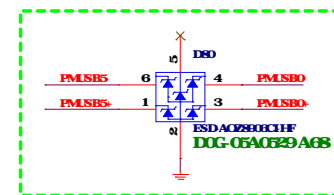
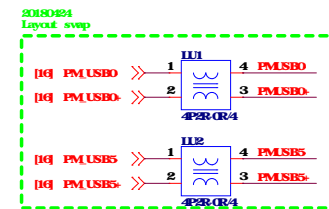
layout note:  av: 10G-430010-114
C21 must close to TVS pin5
TVS must near HBM1 connector and route without branch
Varistor must close to TVS and route without branch

TYPE A H3EQ1004 Redriver

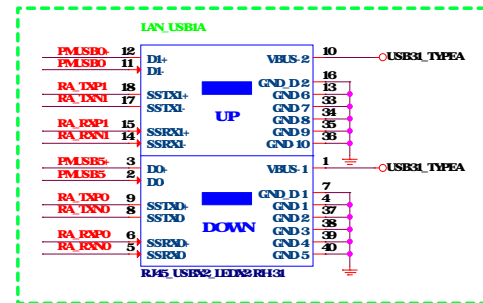
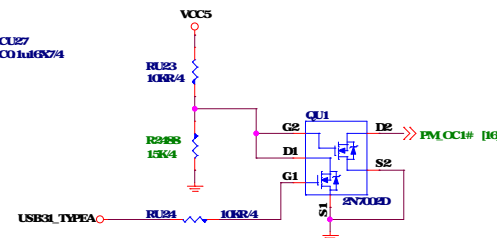
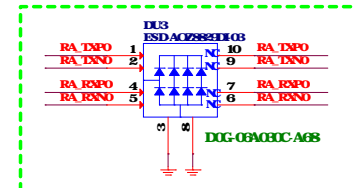


EQ	dB	
0	10 9	0 to GND
R	6 7	68K to GND
F	8 9	NC
1	13 1	0 to VD

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VID



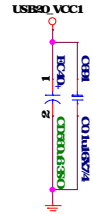
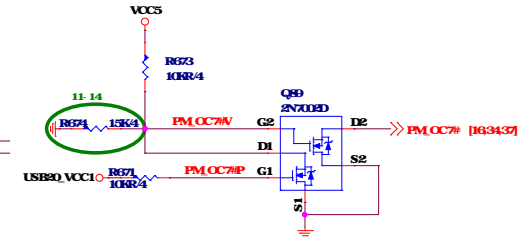
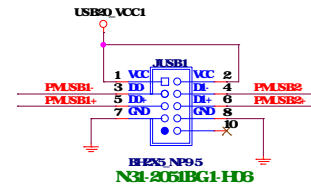
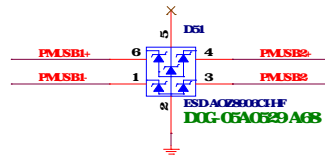
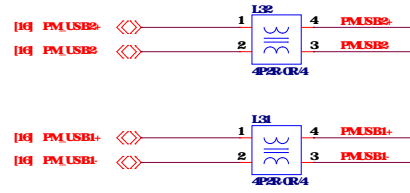
close to Type A Connector



20180409
Change to N58 32F0721- F02

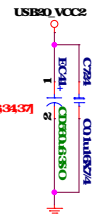
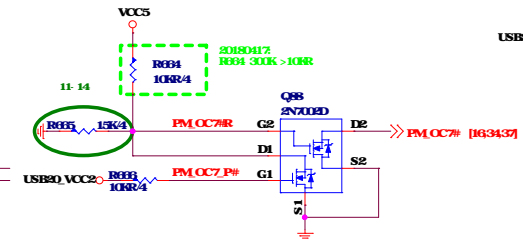
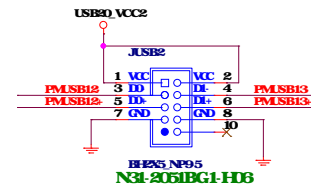
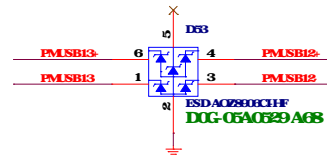
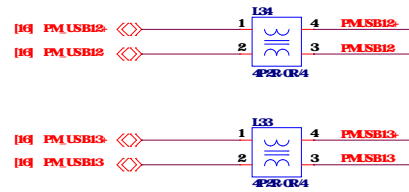
Front USB2 Q (JUSB1)

5V@1A

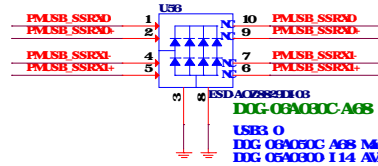
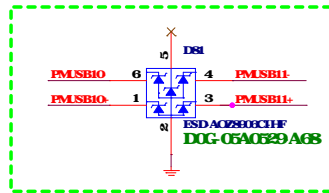
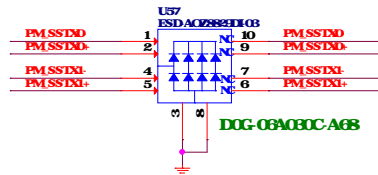
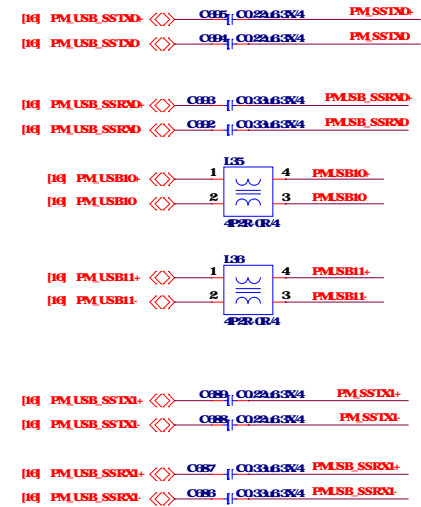


Front USB2 Q (JUSB2)

5V@1A

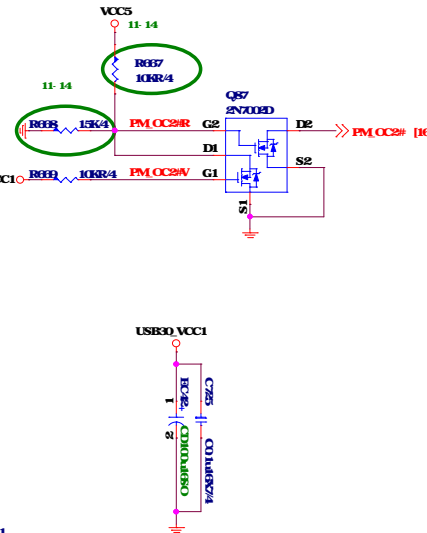
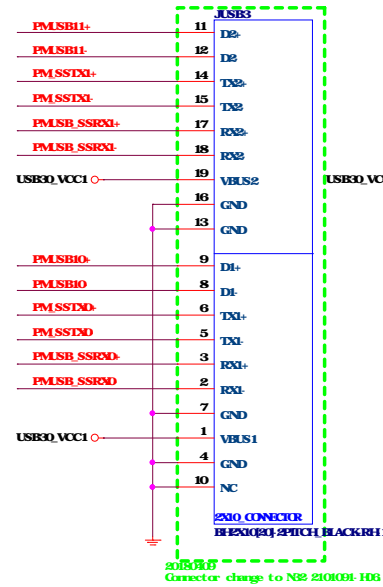


Front.JUSB3 5V@1.8A



USB3 0
DIO 06A050C A68 Mil n
DIO 06A050D 114 AM.

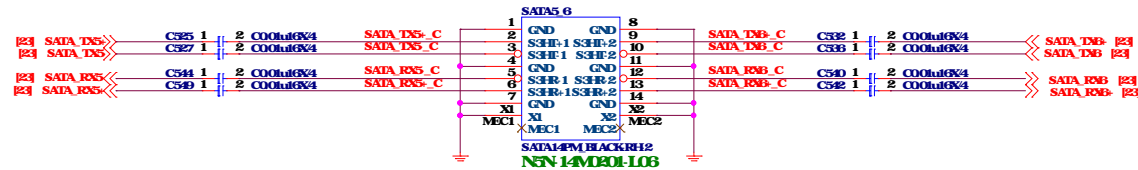
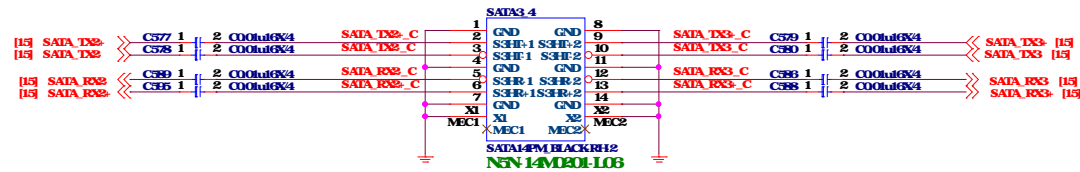
USB2 0
DIO 0800529 A68 Mil n
DIO 0800519 105 AM.



SATA Connector

20180427

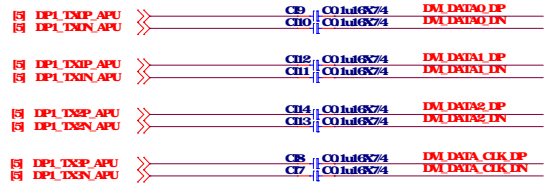
SATA1 SATA2 connector change to 180 degrees.



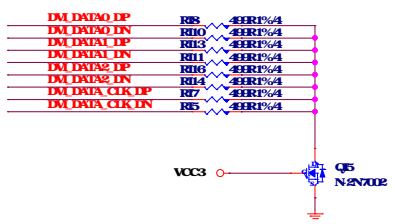
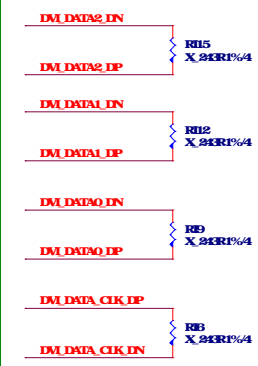
Schematic Cfg		Project	
MS-7869/BEDGAMNGHUS		V	A
MS-7869/BEDAIRO			

MSI <small>Microstar International</small> MICROSTAR INT'L CO., LTD.	
SATA	
Doc Name MS-7869	Rev 2.0
Date Monday, May 14, 2018	Sheet 30 of 68

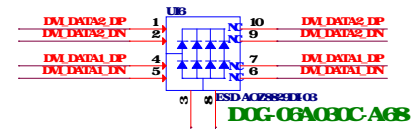
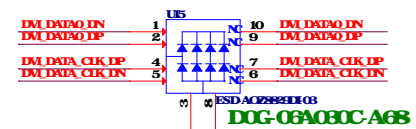
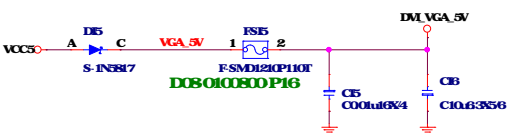
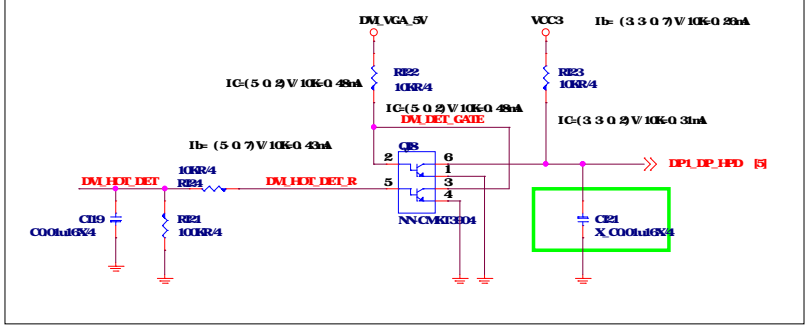
DMI CONNECTOR



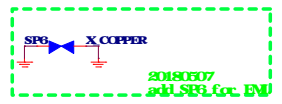
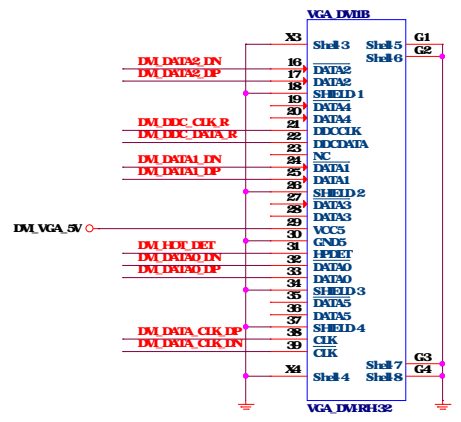
For EM



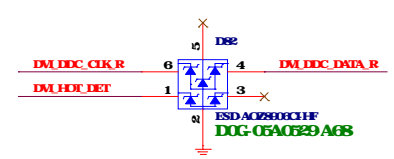
HDD



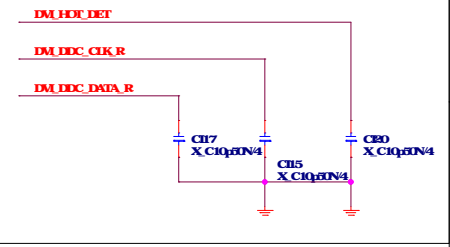
20180102
VGA_DM1B Change to N58 43F011-E8B



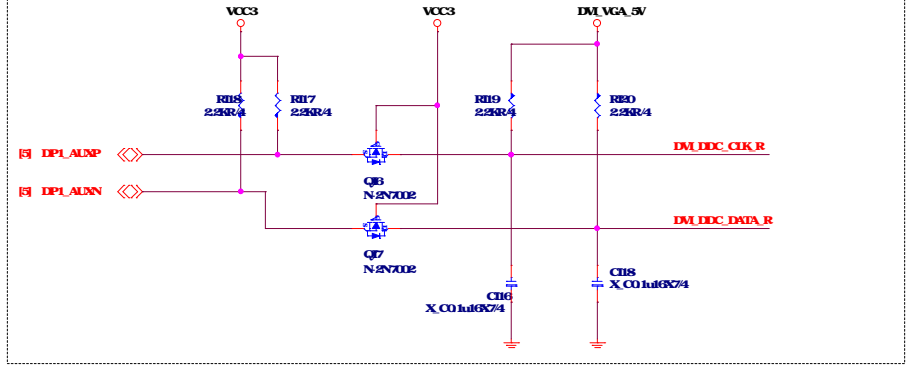
5V



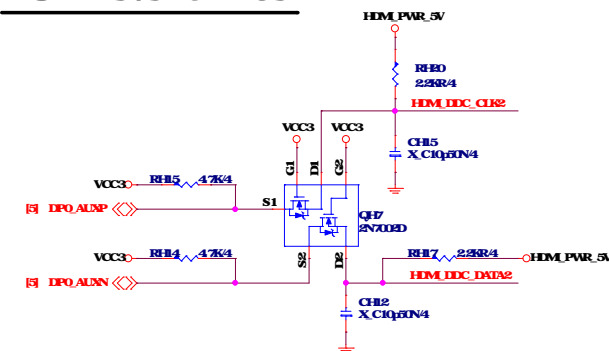
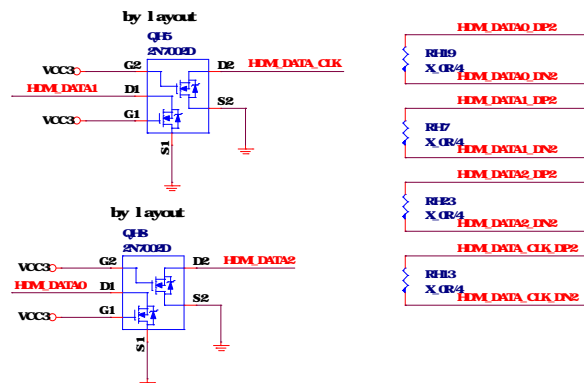
For EM



LEVEL SHIFT using E2C Repeater

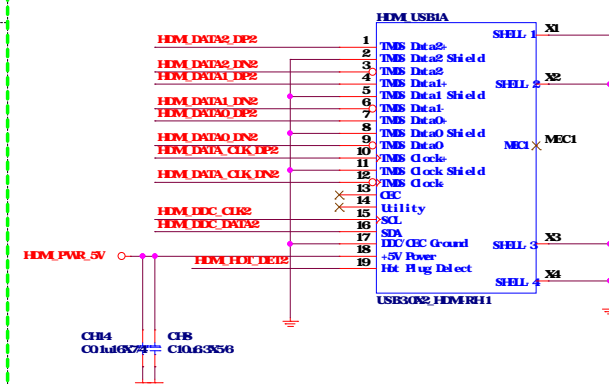


For HDM 1.4

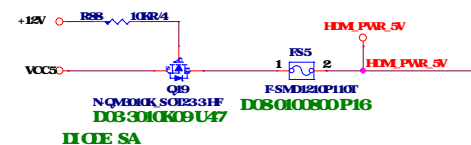
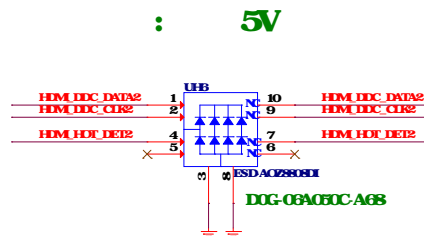
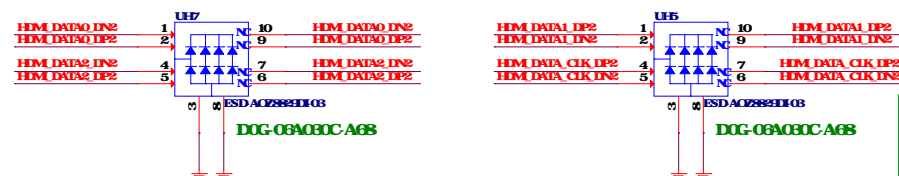


Connector

20180409
Connector change to N58 37M0121- L06



Connector Power

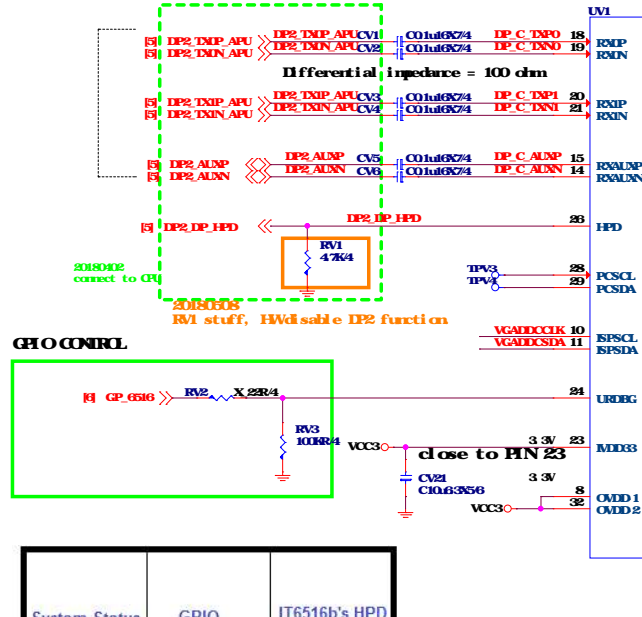
**For EM**

Note

If connect to eDP port, must confirm whether it support hot plug detection on HPD and re-audstraining

7B86 1.0 D Sub

(RV1)



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS M0de	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

If have VSI1.2 SPEC request , You can change bead to L02 220012 M09 use ,It test PASS.

II6516BFX_CX

RV1 stuff, HWdisable DP2 function

GPIO CONTROL

GP.0516 >> RV2 X 22R4

RV3 100R4

VCC3 3.3V

close to HN23

CV2 C10.6356

VCC3 3.3V

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

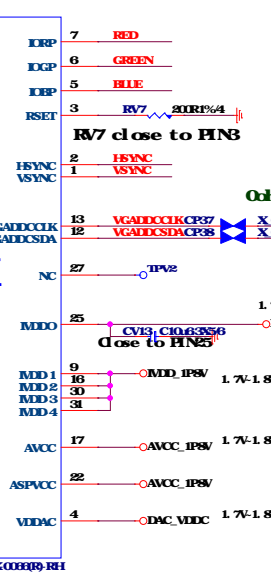
OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2

OVDD1 OVDD2



0ohm COPPER

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

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RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

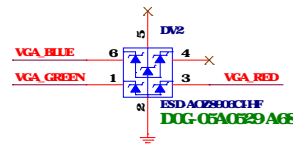
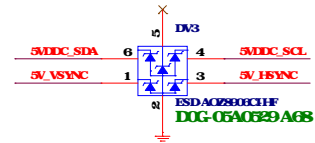
RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

RV7 close to HN3

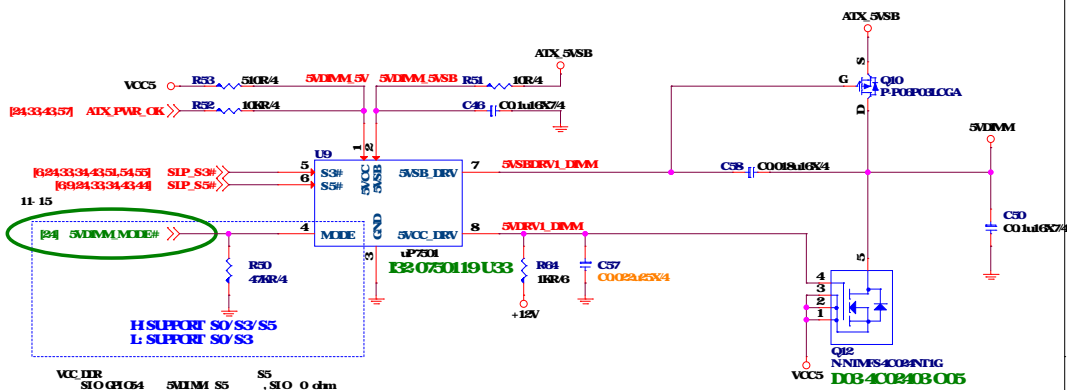


remove 3.3V to 5V level shifter (0301)

RV11 RV12 100 ohm change to 22 ohm (0301)

Vendor suggest 22ohm for better I2C quality

5V DIMM FOR DDR



3VSB cost down

3 3V@2 695A **CCP=3 8A**

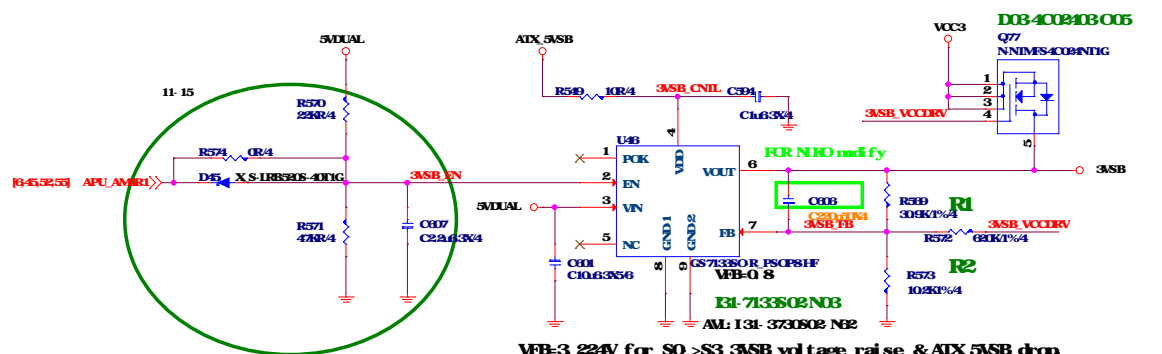
1.05V@0.05A**VDDBT_RTC G@4.5uA**

FCH@Q 07A

CPU@Q 25A

VDDIO AUDIO@0.278A

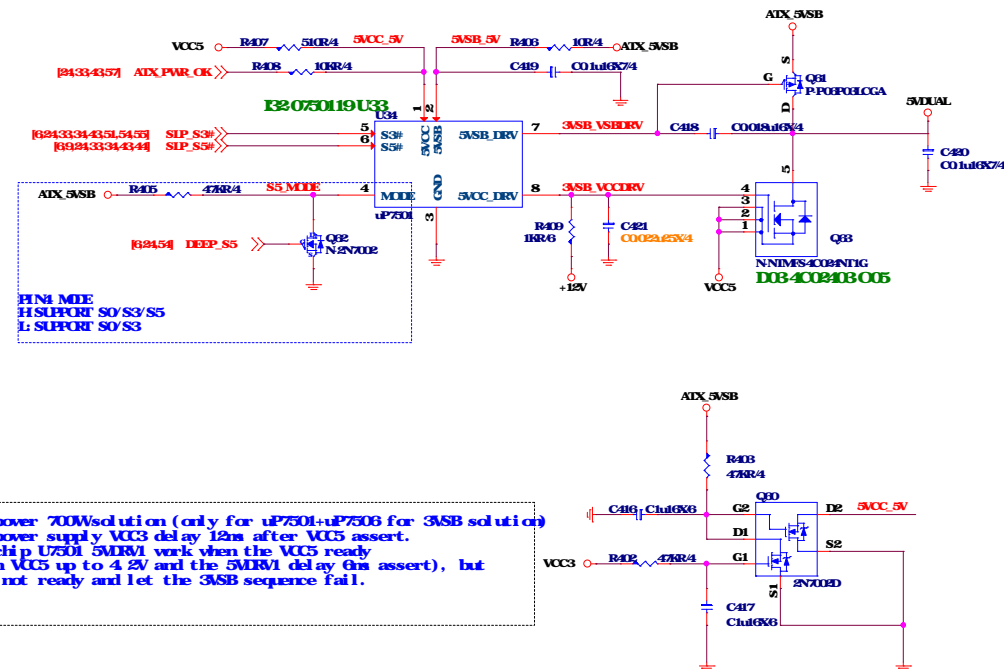
PQE*6 @225A



VB=3 224V for S0 >S3 3VSB voltage raise & AIX 5VSB drop

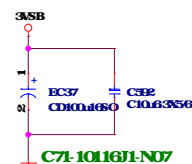
$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

5VDUAL For 3VSB CPU 1.8V VDDP

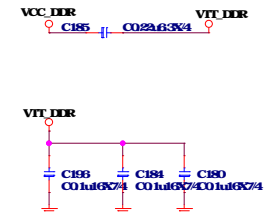
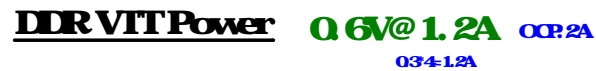


For power 700W solution (only for uP7501+uP7508 for 3ASB solution)
The power supply VCC3 delay 12ns after VCC5 assert.
The chip U7501 5VDRM1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRM1 delay 6ns assert), but
VCC3 not ready and let the 3ASB sequence fail.

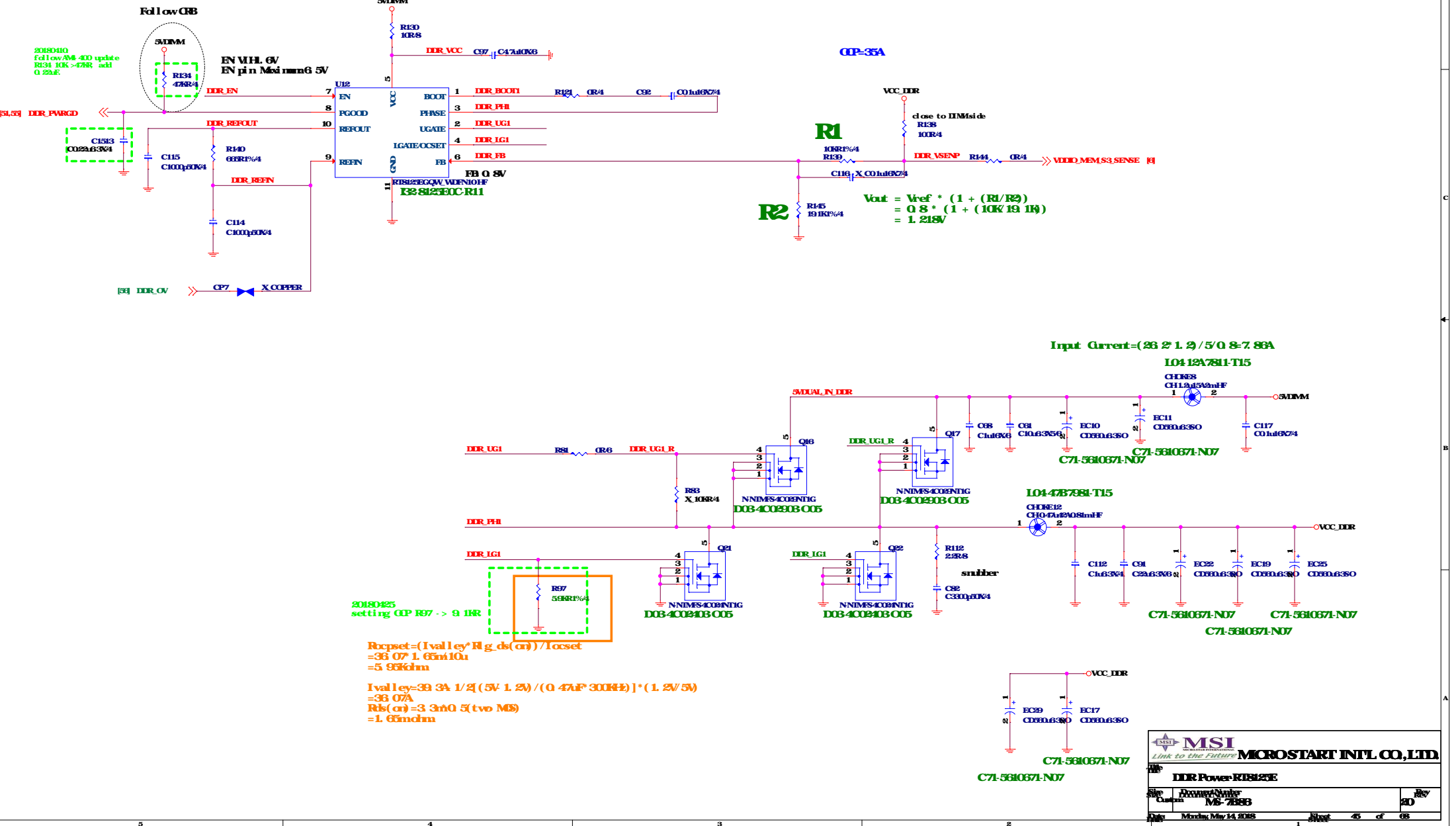
2 695A

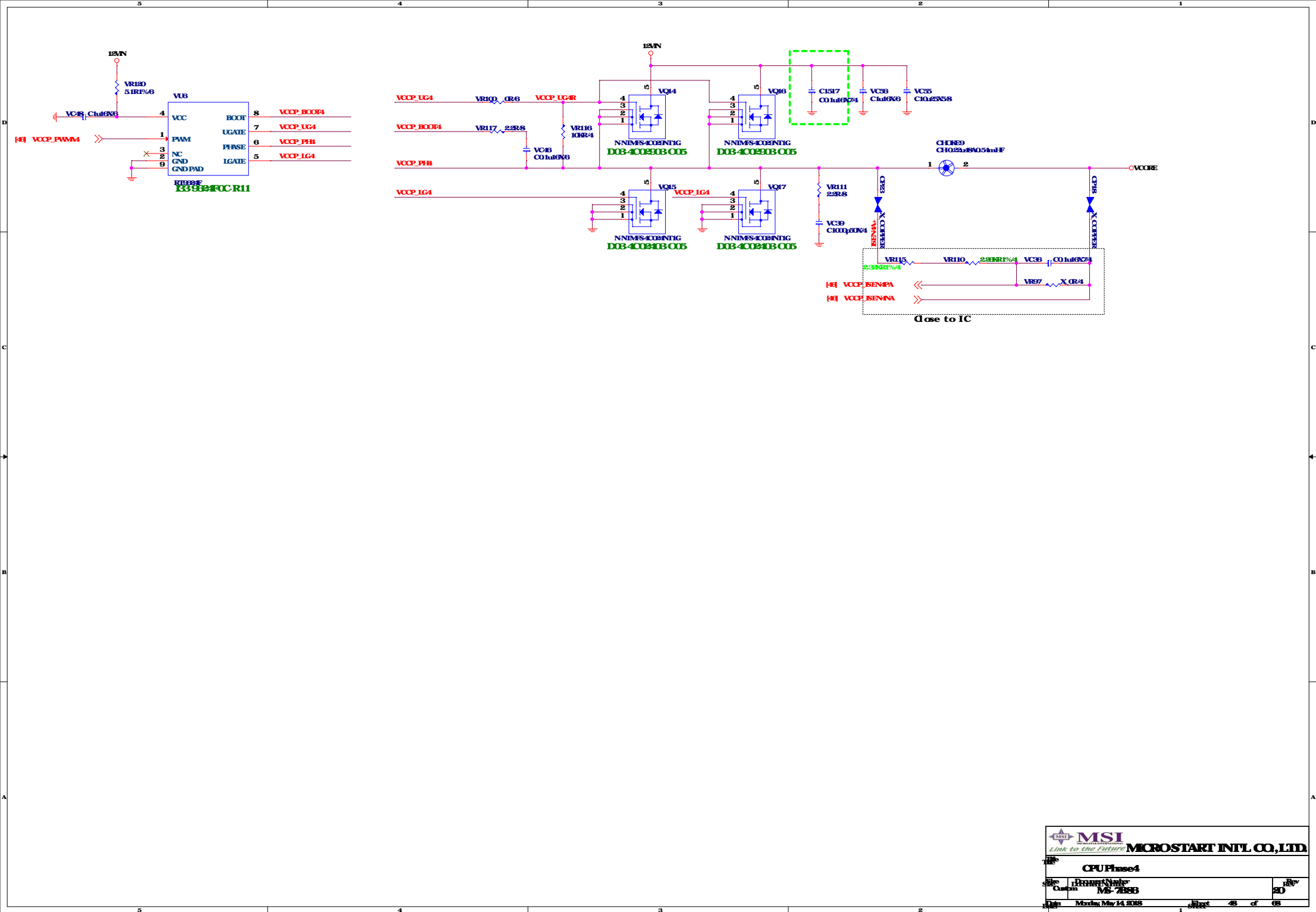


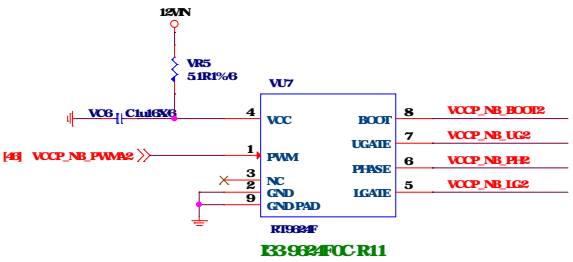
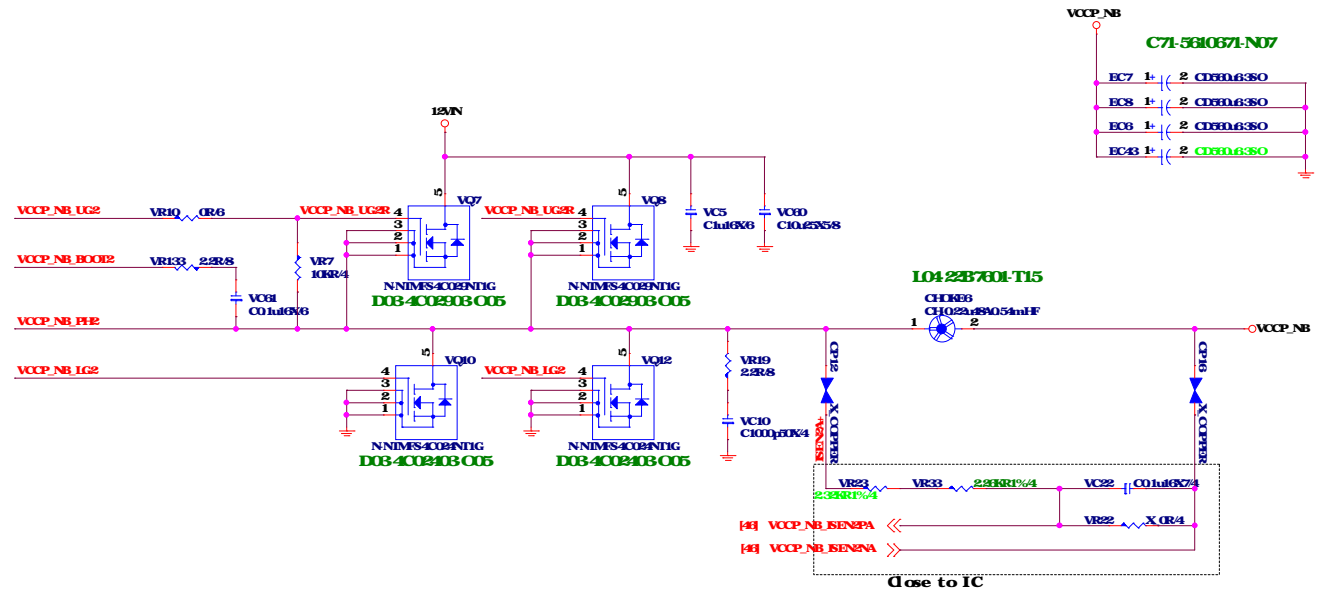
25V@2.24A OCP:4A



DDR4 1.2V@26.2A
15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT
Rocset: 8.06K
OC= Rocset * 10uA/Rbscn(Low side * 2)
= 5.9K 10uA/ 1.65mhm
= 35.75A





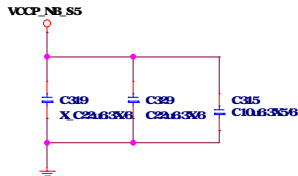
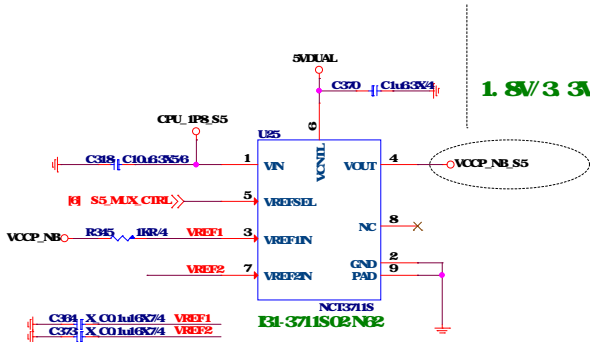
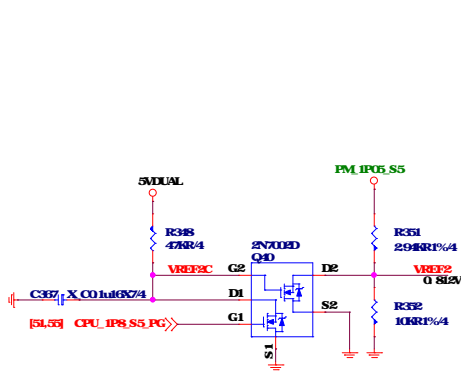


FOR VCCP_SOC_S5 CPU=2A

1. 8V/ 3.3V@900mA

S5_MUX_CTRL:
H S0 > +VDDCR_FCH_ALWv11 track VDDNB
L: S3/S5 -> If VDDCR_SOC=0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V
If VDDCR_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 v11 track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h 6Fh processors)



[S4:35:02:5] TYPE1_CPU_SEL >>

TYPE1_CPU_SEL:
0 TYPE 0
1 TYPE 2

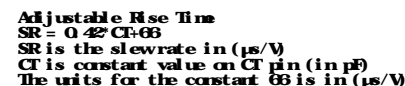
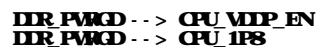
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP NB S5)



1. 8V@2A **CCP-6A**



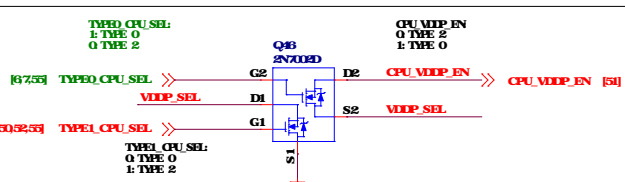
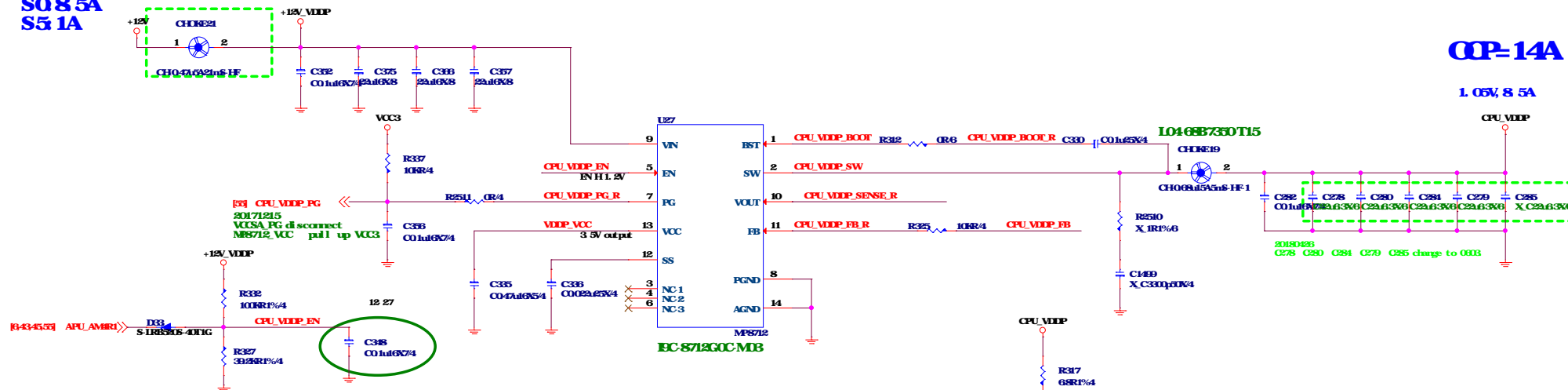
CPU_VDDP_S0

1.05V/0.9V@S0.85A
S0.85A
S5.1A

Input Current = (8.54 * 1.05V) / 12V = 0.8-0.93A

COP-14A

1.05V, 8.5A



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	1
NA	1	0	0	0
SR	2	1	1	CPU VDDP NOT SUPPORT TYPE2
R/ZP	3	0	1	1

TYPE1_CPU_SEL
0 Type 0/1 => 1.05V
1: Type 2/3 => 0.9V
[5635509253] TYPE1_CPU_SEL

FMCHOR9
Page 17 pull high
1: Type 0/1 1.05V
0 Type 2/3 0.9V

Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2/R3)))$
 $= 0.6 * (1 + (1K/(2K/3.83K)))$
 $= 1.05V$

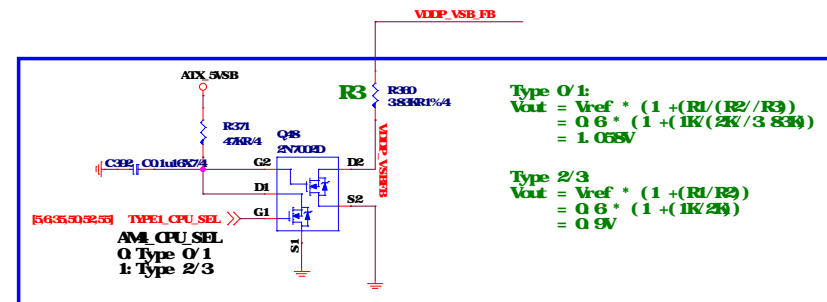
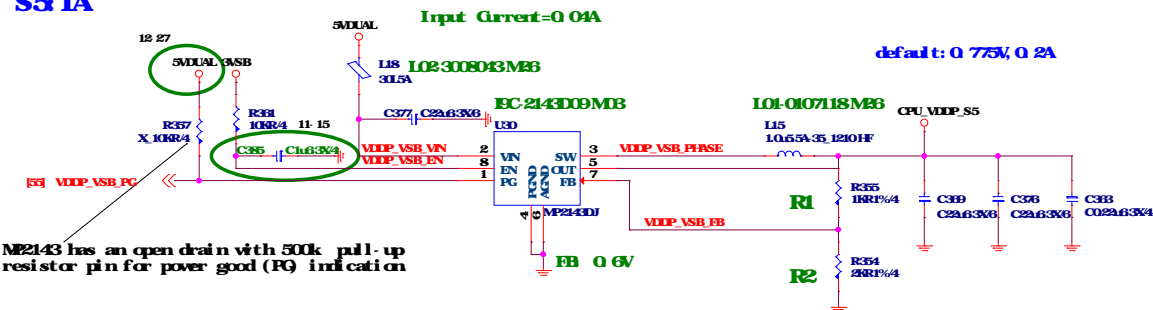
Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$

CPU_VDDP_S5

1.05V/0.9V
S5.1A

Input Current = 0.04A

default t: 0.775V, 0.2A

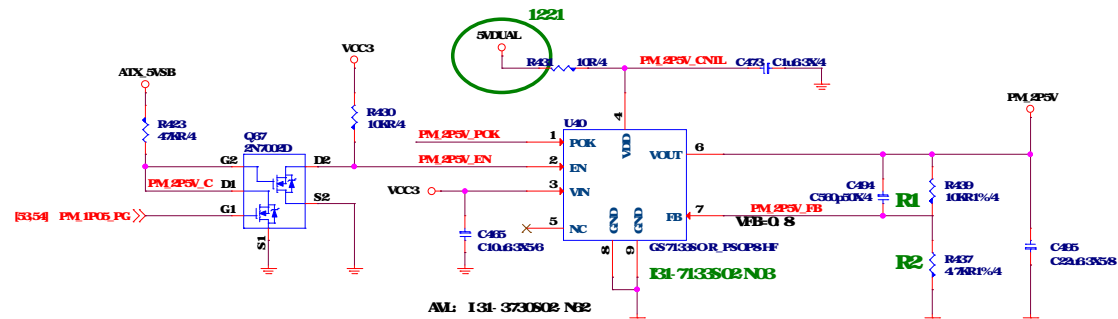


Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2/R3)))$
 $= 0.6 * (1 + (1K/(2K/3.83K)))$
 $= 1.05V$

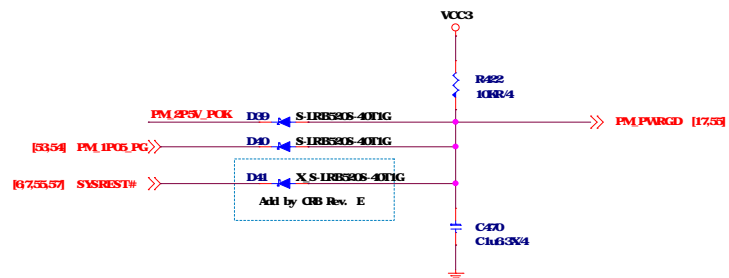
Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$

MP2143 has an open drain with 500k pull-up resistor pin for power good (PG) indication

2.5V@900nA **OP-3.8A**

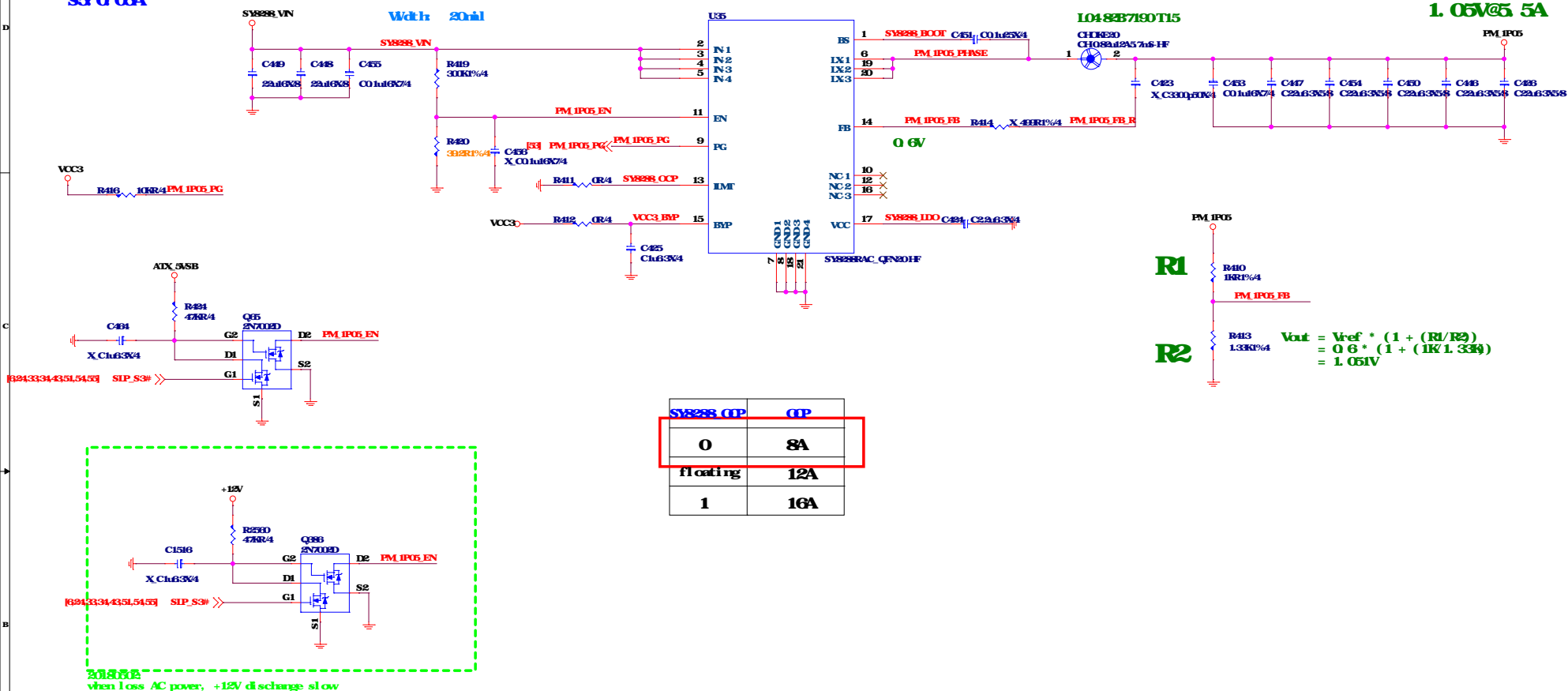


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/4.7K)) \\ &= 2.502V \end{aligned}$$



1. 05V
S0 5 5A
S5 0 05A

Input Current = $(5.5A \cdot 1.05V) / 12V = 0.8 \sim 0.6A$

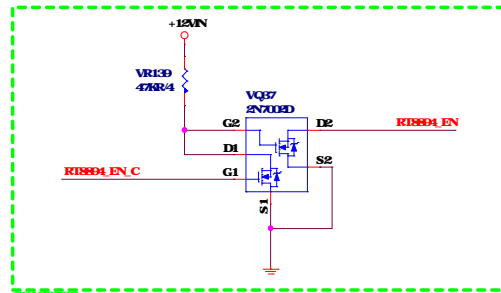


1.05V@0.05A
0.05A FOR VSUS105

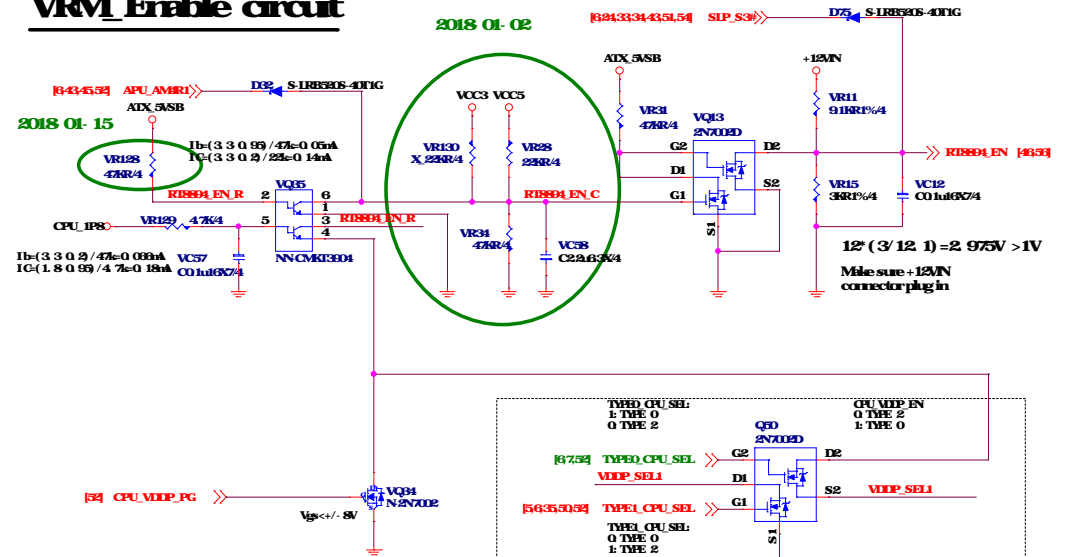
[illegible]

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (1K/3.16K)) \\ &= 1.05V \end{aligned}$$

VRM Enable circuit



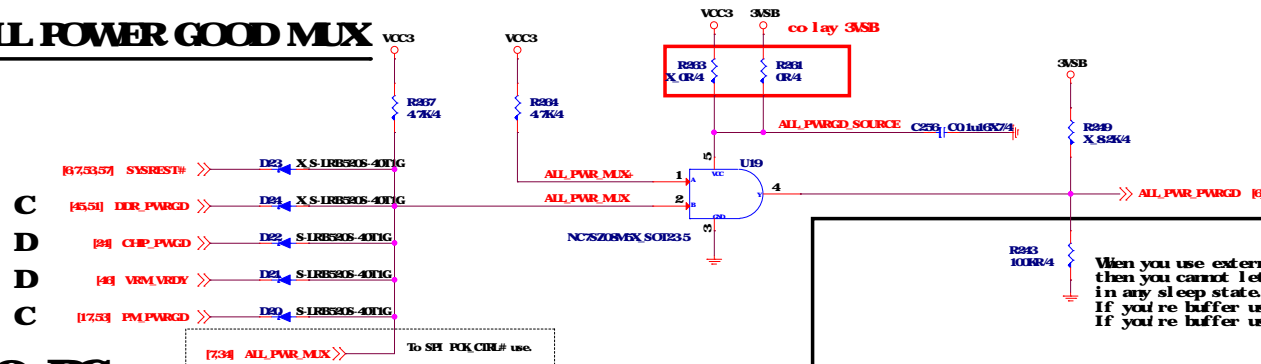
2018 01-15
when loss AC power, +12VIN discharge slow



CPU VDDP NOT SUPPORT TYPE2

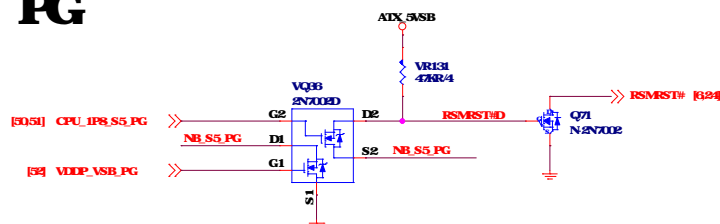
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/TP	3	1	0

ALL POWER GOOD MUX

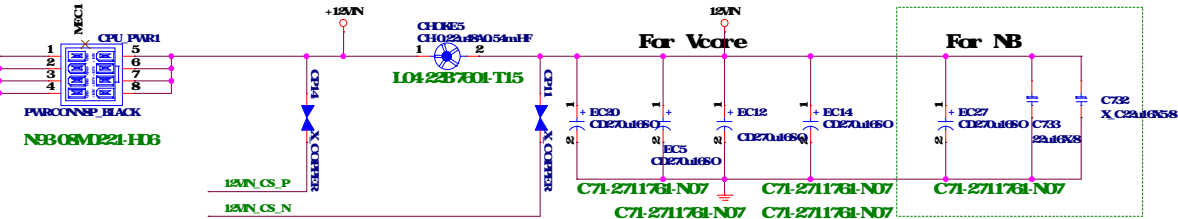


When you use external buffer then you cannot let APU PWR_GOOD pin float in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K.
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG
S5 PG



CPU POWER CONNECTOR



NB		VCCP	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 1.4	> output Vcore	Vout = 1.4	> output Vcore
D = 0.116667		D = 0.116667	
Io = Icoremax*0.8		Io = Icoremax*0.8	
I core(max) = 75	> Vcore current	I core(max) = 125	> Vcore current
I avg. = 75	A	I avg. = 125	A
I ripple (Io / D* / (1-D)) / Phase		I ripple (Io / D* / (1-D)) / Phase	
Phase = 12	phase	Phase = 12	phase
I ripple = 12.03835	A	I ripple = 10.03196	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 5000	m A	I ripple(cap) = 5000	m A
COEmax = 1		COEmax = 1	
Input Cap. = 3	pcs.	Input Cap. = 3	pcs.

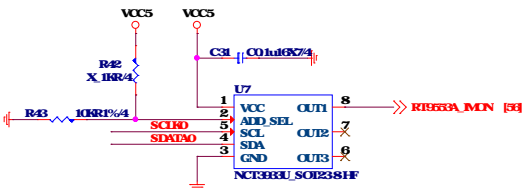


Over Voltage Control IC

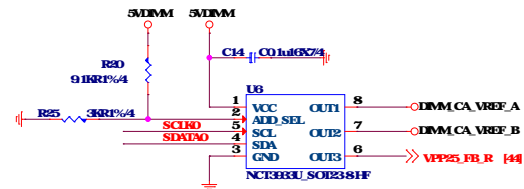
UV VOLTAGE CONTROL

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH(40hm)	OPEN	39	3	22	13	10
RL(40hm)	10	13	23	3	39	OPEN
BUS_SEL	0%	23%	40%	60%	73%	100%

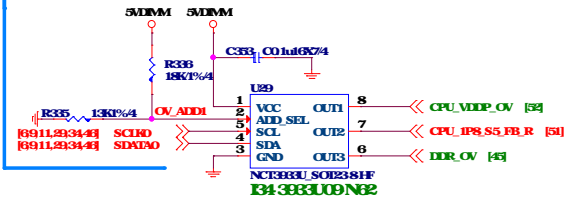
0x2A RH=OPEN RL=10K



0x28 RH=1K RL=3K

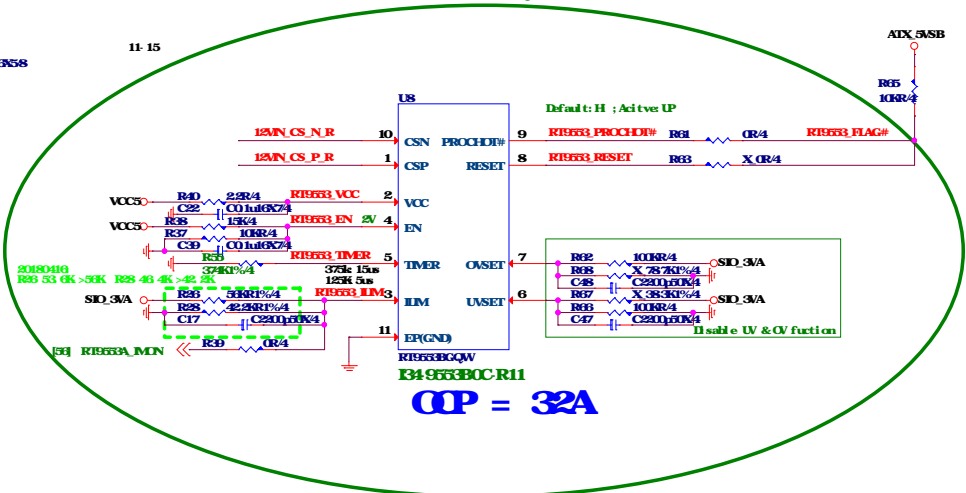


0x26 RH=18K RL=13K

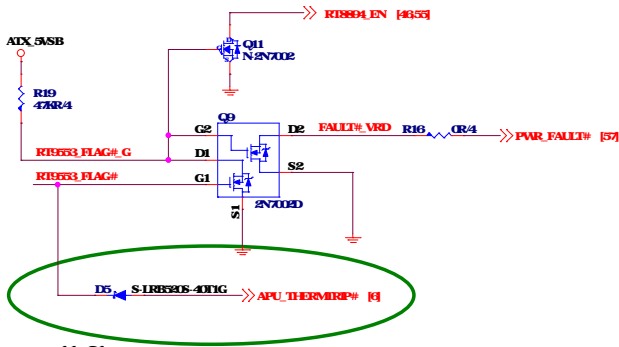
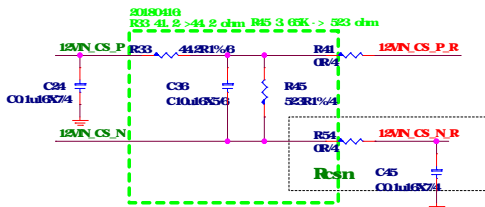


RI9553B CURRENT SENSE

RI9553 PIN5 When start OV/UV, RESET delay time can meet SPEC 15us.

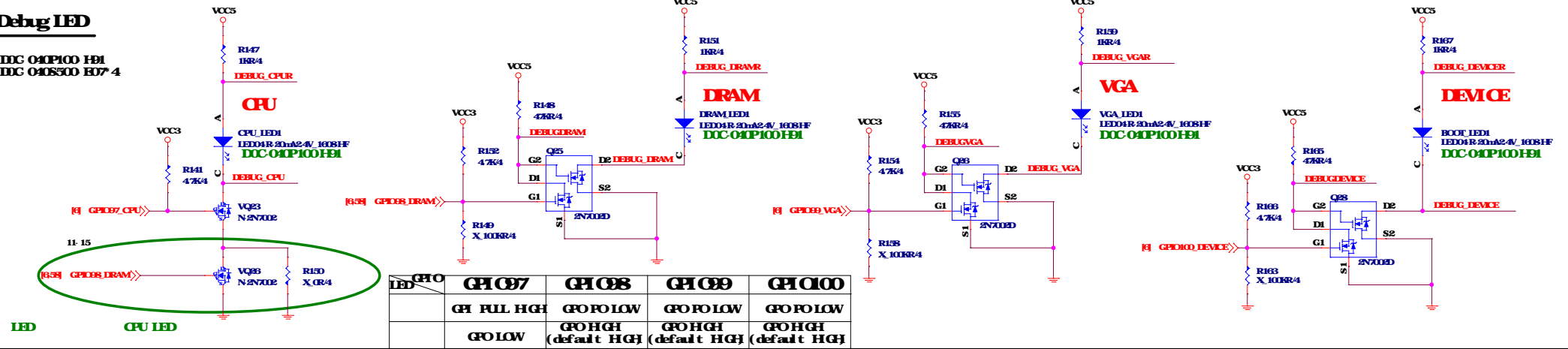


COP = 32A

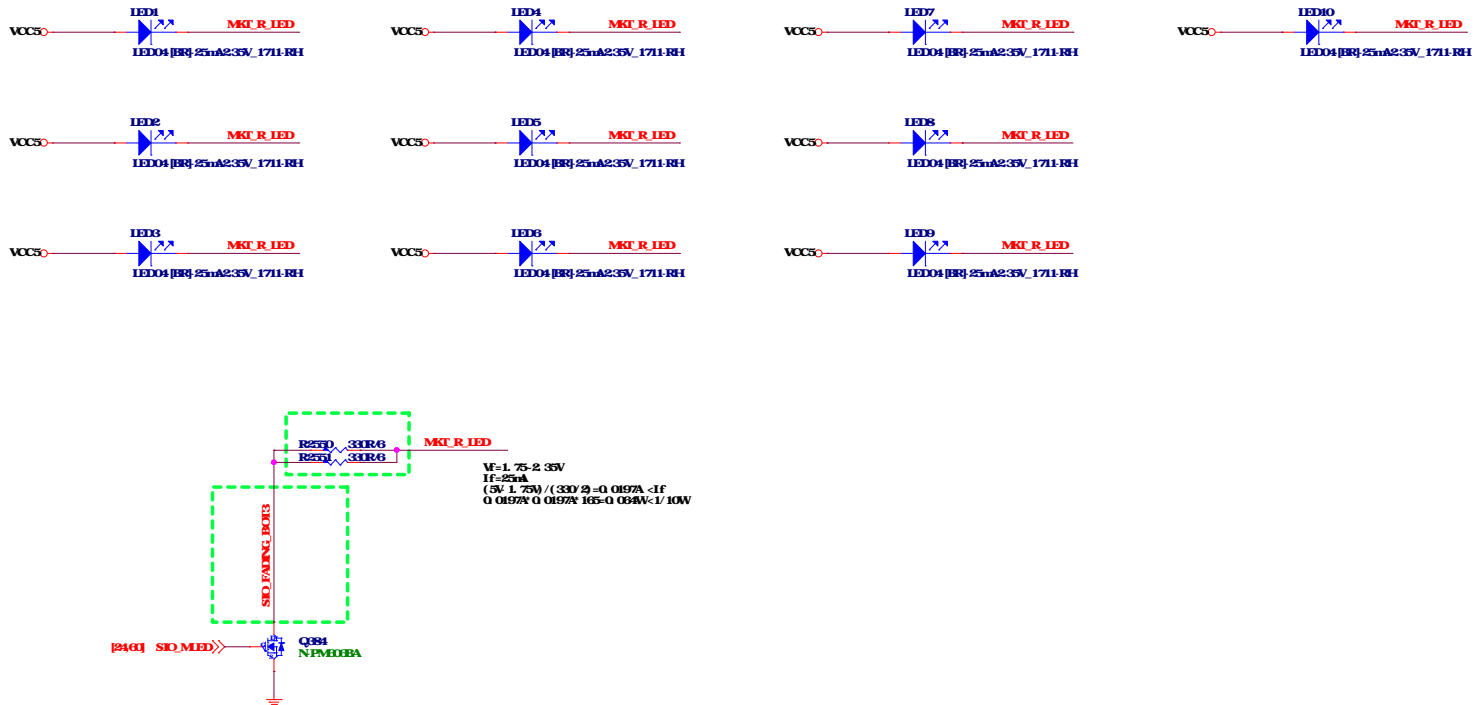


EZ Debug LED

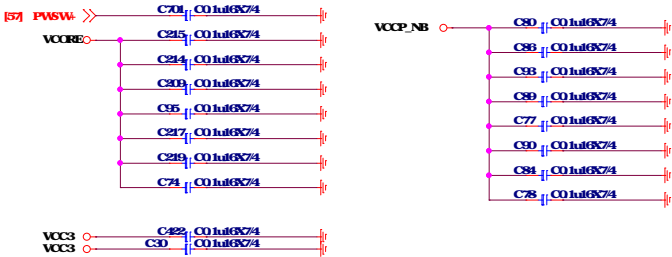
: MDDG 040P100 H01
S: DDG 040S500 E07* 4

**MKT Name LED x10**

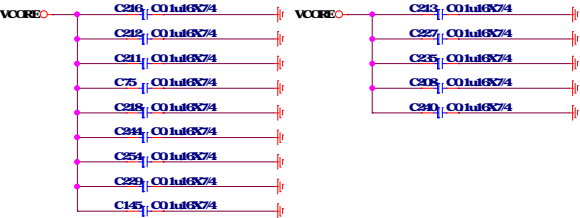
LED "GAMING PLS"



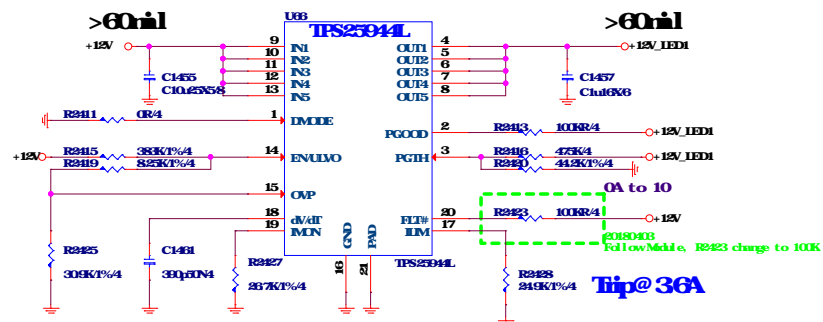
Add for EM



return path



JRCB1

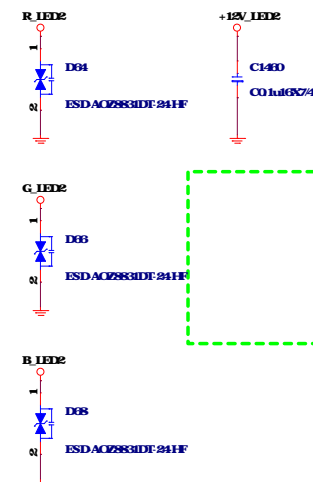
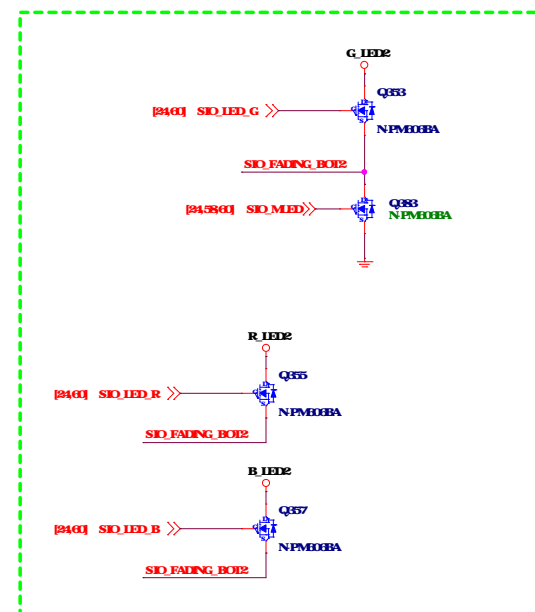
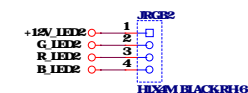
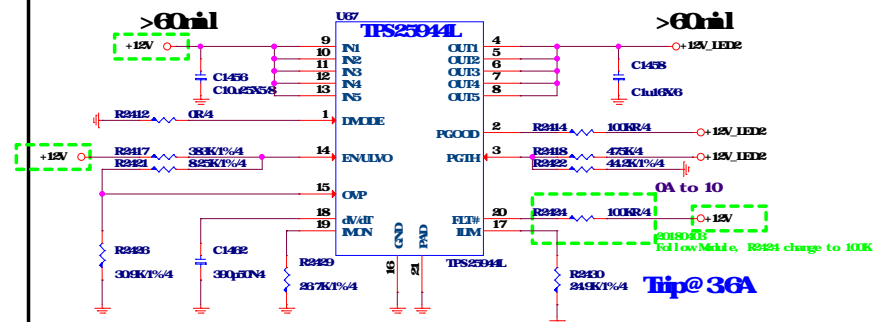
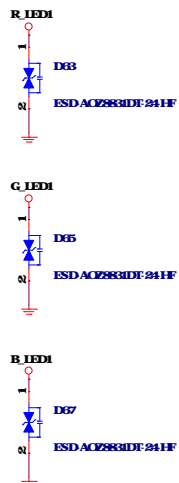
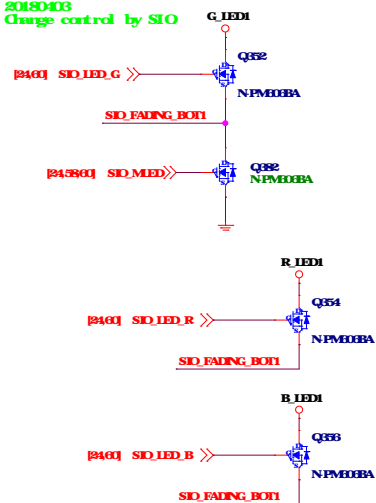
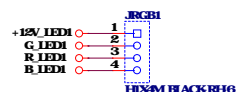


Color	SIQLED R	SIQLED G	SIQLED B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

SIO 3VA



PMSPEC Default WHITE Color




LED (RGB) (JRGB2) 5050 RGB LED (12V/G/R/B) , 3 (12) ,

LED (RGB) (JRGB)
 --- RGB
 --- RGB 5050 RGB LED (12V G/R/B) , 3 (12) ,
 2

5 4 3 2 1

BOARD SIDE LED*6

20180426
FMSPEC cancel board side LED



MSI
MICROSTAR INTERNATIONAL
Link to the Future

MICROSTAR INT'L CO., LTD.

Title

BOARDSIDE LED

Size	Document Number	Rev
Custom	MS-7883	20
Date	Monday, May 14, 2006	Sheet 61 of 68

OPTION BOM PARTS

60 Level

	A	B	C	D	E
PCIEX16 SLOT	OPT PCIEX16.1 PCIEX16 SLOT_PCIEXP104_18P N11-16H821-L03	OPT PCIEX16.2 PCIEX16 SLOT_PCIEXP104_18P N11-16H811-L03			
PCIEX8 SLOT	OPT PCIEX8.1 PCIEX8 SLOT_PCIEXP100_7P N11-1000331-L03	OPT PCIEX8.2 PCIEX8 SLOT_PCIEXP100_7P N11-1000321-L03			
REAL USBType A					
SOLIDCAP 270uF6					FOOTPRINT C/P2 5.D8.3.H2 C/P3 5.D8.H0 C/P3 5.D8.H8
SOLIDCAP 560uF3					FOOTPRINT C/P2 5.D8.3.H0.5 C/P2 5.D8.3.H0
SOLIDCAP 470uF3					FOOTPRINT C/P2 5.D8.3.H0.5 C/P2 5.D8.3.H0
SOLIDCAP 100uF6					FOOTPRINT C/P2 5.D8.3.H0 C/P2 5.D8.3.H6
MEM SLOT	OPT MEMVRED1 MEMSLOT DDR4/D88 N13-2880701-L03	OPT MEMVRED1 MEMSLOT DDR4/D88 N13-2880681-L03			FOOTPRINT DDR4/D88_1.T DDR4/D88
MTG Label					
PCI SINK					
MOSN +IO					
MOSW					
FS2_USB	OPT FS2_USB.1 FS2_USB IOASM_USB_DIN14 N5B-14M0241-H03	OPT FS2_USB.2 FS2_USB IOASM_USB_DIN14 N5B-14M0221-H03			
HDM_USB	OPT HDM_USB.1 HDM_USB IOASM_USB3_HDM37 N5B-37M0121-L03	OPT HDM_USB.2 HDM_USB IOASM_USB3_HDM37 N5B-37M0101-L03			
LAN_USB	OPT LAN_USB.1 LAN_USB IOASM_RJ45_USB_LED32 N5B-32F0721-F02	OPT LAN_USB.2 LAN_USB RJ45_USB32_LED32_1000R1 CN5-7B23001-F02			

5010 Level


	A	B	C	D	E
PCI					
M2SLOT					FOOTPRINT SLOT_NFFROMB7_3H SLOT_NFFROMB7_2
VGA+DMI	OPT VGA_DMI.1 VGA+DMI DMI_CONN_8P_17P N5B-24F0821-EB6	DMI	OPT VGA_DMI.2 VGA+DMI DMI_VGA IOA_VGA_DMI_43P N5B-43F0111-EB6		FOOTPRINT IOA_VGA_DMI_43P DMI_CONN_8P_17P
PCI	OPT PCI.1 PCI P40-07B8810-G37	OPT PCI.2 PCI P40-07B8830-G37			
0Ohm (0402)					
LED	OPT LED_LED_5010.1 LED LED5_19.2SYCC DCC-040P100-H91	OPT LED_LED_5010.2 LED LED5_19.2SYCC DCC-040E200-H91			

5020 Level

	A	B	C	D	E
LED					

60 Level

	A	B	C	D	E
Audiocover					
AudioJack	OPT AUD JACK.1 Audio Jack AUDIO_JACK8_8P_U2 N54-26F0381-L03	OPT AUD JACK.2 Audio Jack JACK_AUD_8P N54-26F0351-L03			
M2SCREW					
PCIEX4 SLOT					

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BOMOption			
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HS3
[REDACTED]
OE3 7B86008 K08
OE3 7B86008 K08

E95 000022 C22

X_B3

SME

X_PNI*2

X_B4

SME

X_PNI*2

AM:
DD6 0100161- F52
DD6 0100101- K23

UEFI
Label
UEFI HCS
G51-MISPPXA-A09
G51-MISPPXA-A09

1.0 **havri t** **MKT name label, use MKT LED**

HDM1A1
[REDACTED]
Y01-RHDM03000
Y01-RHDM03000

GAMING Only


MTG1

Label
MTG.NNE

G51-MISPN15 Q13

NAHMC
[REDACTED]
Y02MU00100NAH
Y02MU00100NAH

GAMING Only

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Link to the Future			
Title Manual Parts			
Size Custom	Document Number MS-7288	Rev 2D	
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